Grand Challenges in RF & Plasmas For Next-Generation Semiconductor Manufacturing

Sandeep Mudunuri, EPG, Lam Research
Hema Swaroop Mopidevi, EPG, Lam Research
Benjamin Yee, DPG, Lam Research

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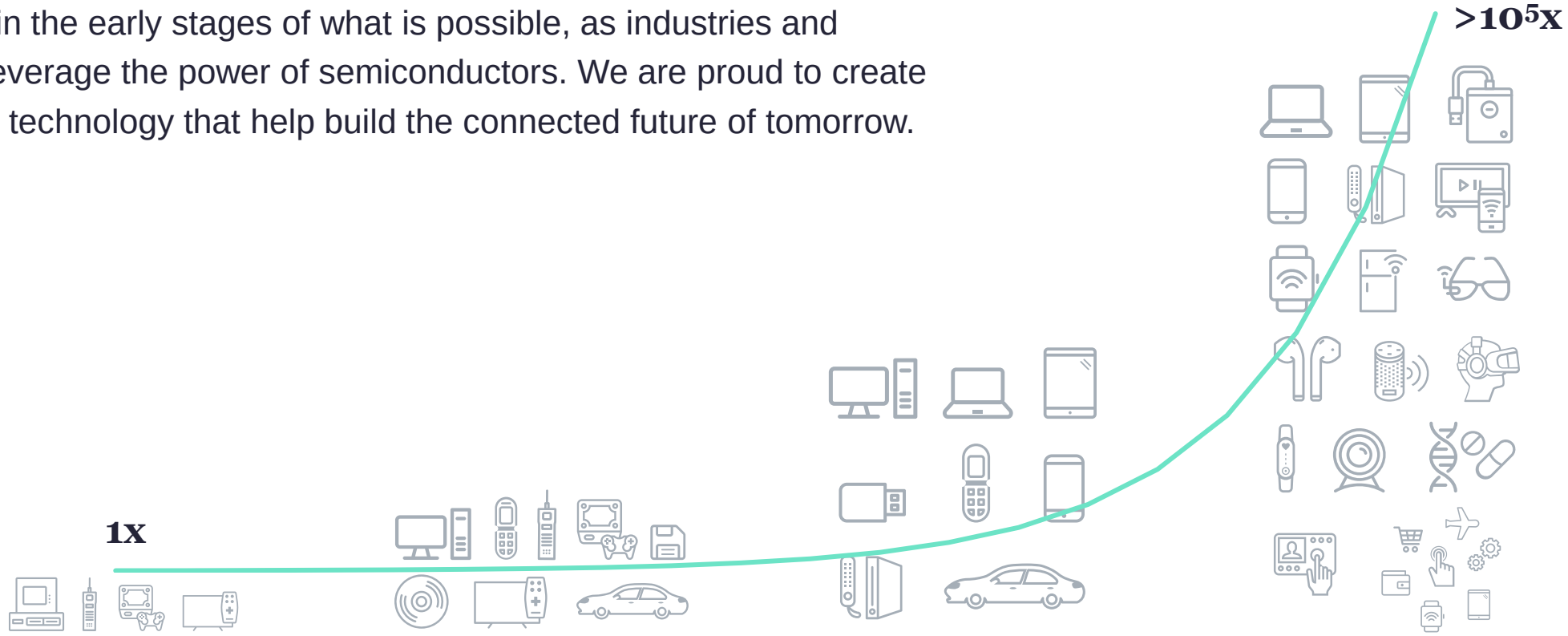
Lam RESEARCH

01

Introduction to Lam Research & Challenges in Etch

Semiconductor demand is intensifying as electronics are increasingly integrated into every aspect of our lives

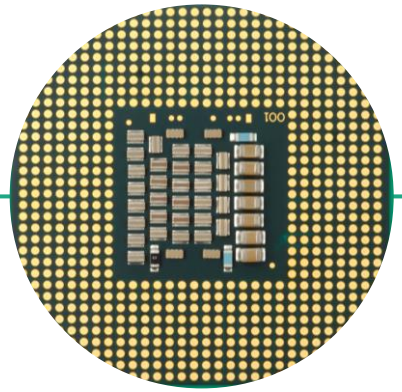
We are only in the early stages of what is possible, as industries and consumers leverage the power of semiconductors. We are proud to create the tools and technology that help build the connected future of tomorrow.



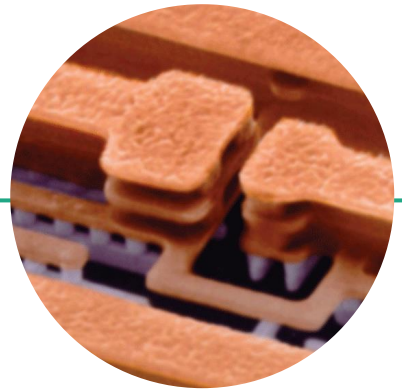
GROWTH IN MEMORY BIT DENSITY AND LOGIC TRANSISTOR COUNTS

Figure not to scale

We are leading the way



At the heart of every electronic product is a complex microchip



Each chip contains thousands of miniature components that require advanced technologies to create

Lam's equipment is used to manufacture these semiconductor devices

Our wafer fabrication equipment is behind virtually every chip on the market.

We play a crucial role in the wafer fabrication process

There are >700 processing steps

Addressed by Lam Research technology

Film placed to be patterned

Pattern mask created

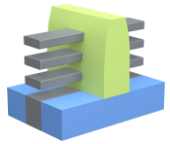
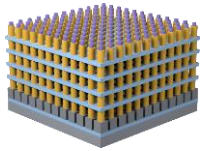
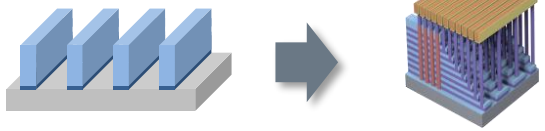
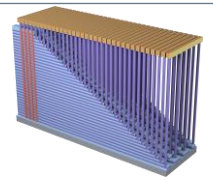
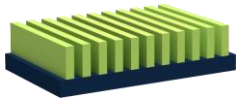
Film selectively removed to define features

Photoresist mask removed

Residues and particles removed

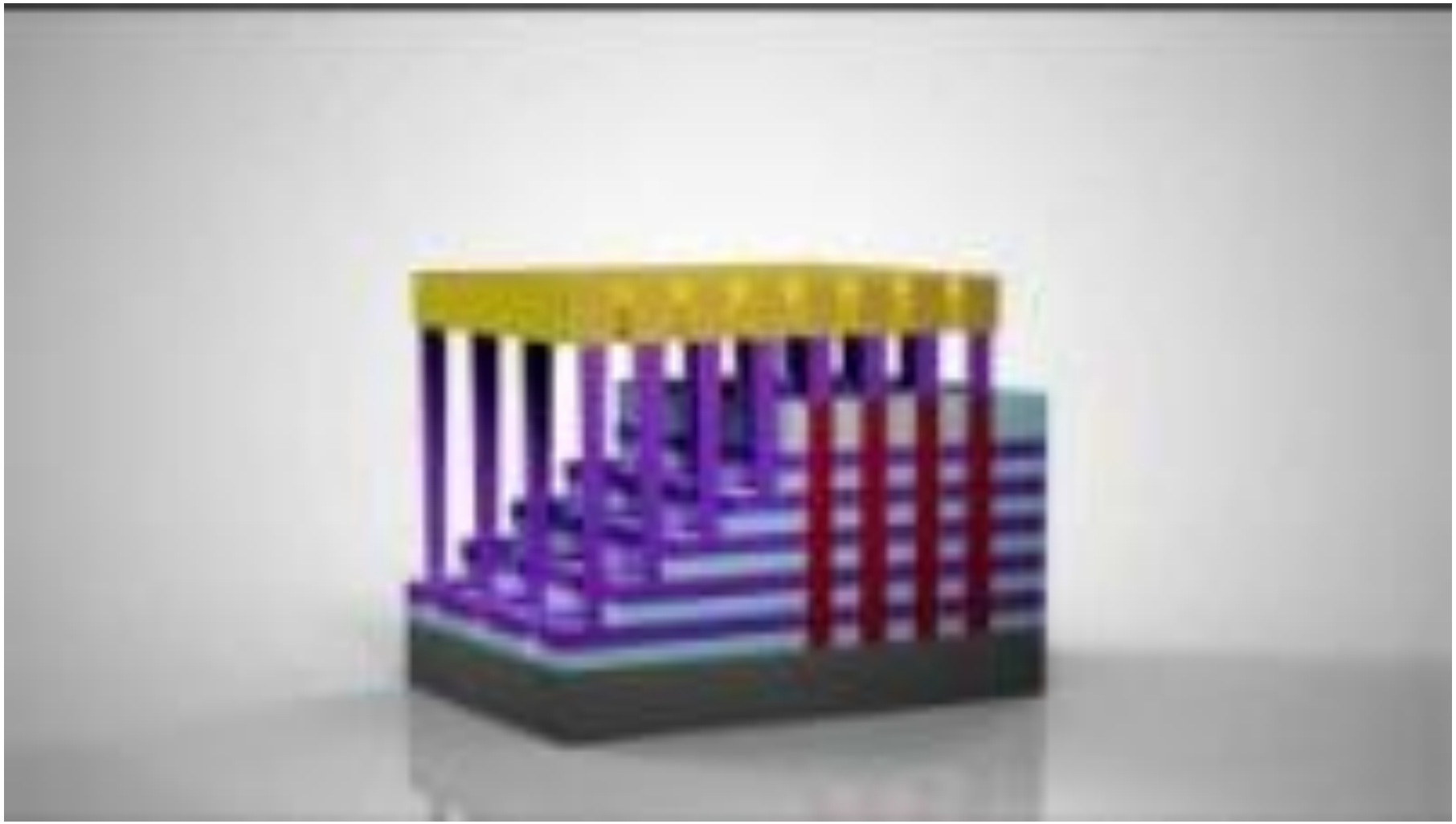
Next materials deposited

Challenges 10 years ago … and today

	PREVIOUS INFLECTION	CHALLENGE	UPCOMING INFLECTION	NEW CHALLENGE
Logic • Performance • Battery life	 Planar FET → 3D FinFET	• Selectivity >3:1	 GAA	• **Lateral precision** • **Selectivity >50:1**
DRAM • Parasitic capacitance • Battery life	 Planar DRAM → Vertical DRAM	• Aspect ratio >60:1 • Profile control	 3D DRAM	• **Aspect ratio >100:1** • **Multiple layers/materials** • **Profile control to >89.96º**
Flash • Data integrity • Density	 Planar NAND → 3D NAND	• Aspect ratio >60:1 • Multiple layers/ materials	 3D NAND +	• **Aspect ratio >100:1** • **Stacking**
Patterning • Density	 Single patterning → Multiple patterning	• CDU <2 nm (3σ) • LWR <4 nm • CD <30 nm	 EUV &Multiple patterning	• **CDU <0.7 nm (3σ)** • **LWR <2 nm** • **CD <10 nm**

CDU= CD uniformity

3D NAND as an example of technology inflections



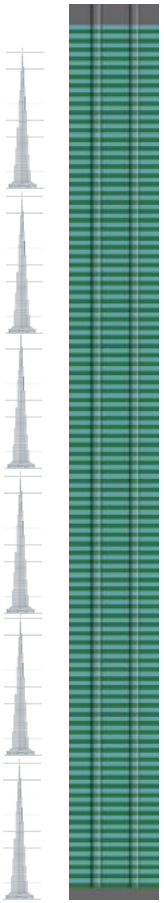
Lam Research: 3D NAND - Key Process Steps

Aspect Ratio is VERY high

Aspect Ratio = 9:1

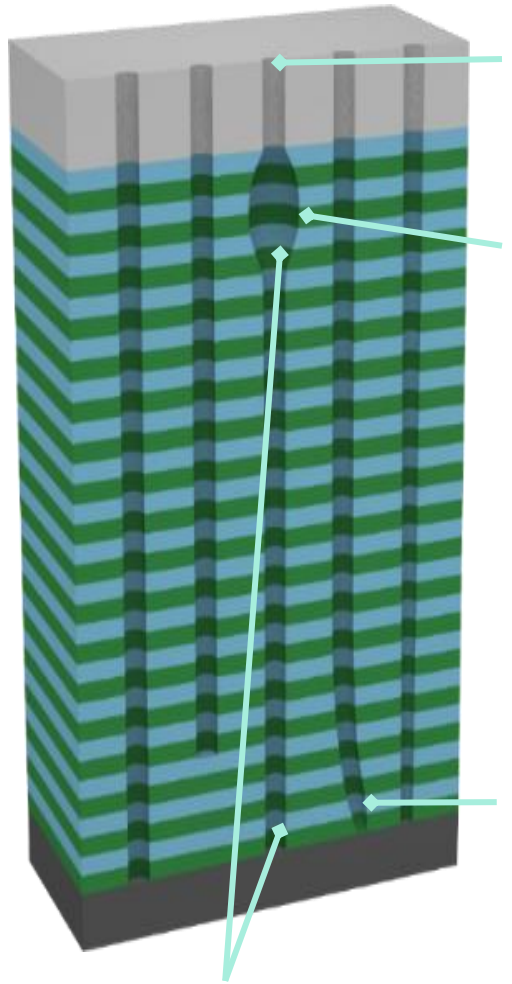
The Burj Khalifa, tallest structure in the world

Aspect Ratio = >60:1



Channel hole etched for 90+ layer 3D NAND

Challenges

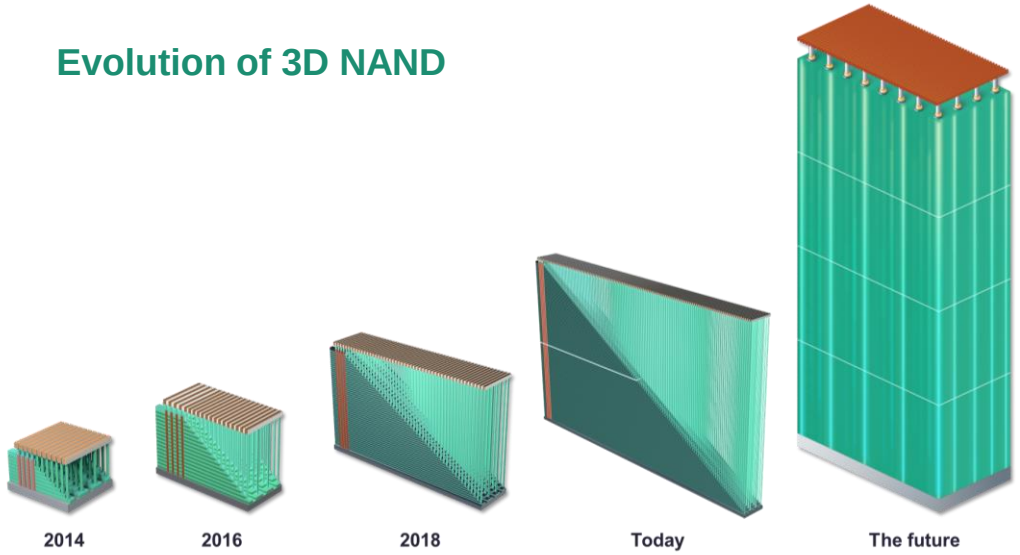


CD delta bow vs. bottom

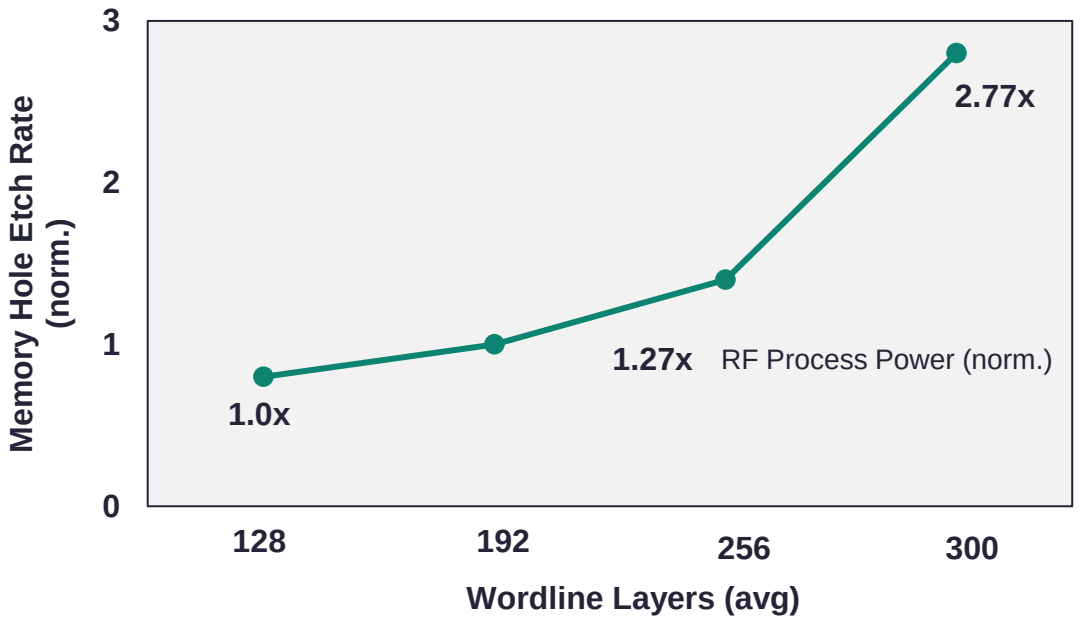
RF Power Scaling for High Aspect Ratio Etching

Memory Channel Etch in 3D NAND requires etching through 100s of layers of silicon dioxide and silicon nitride. A single wafer can have over a trillion channels that have to be etched with near perfect precision

Evolution of 3D NAND



RF Power Scaling for Memory cell etching in 3D NAND



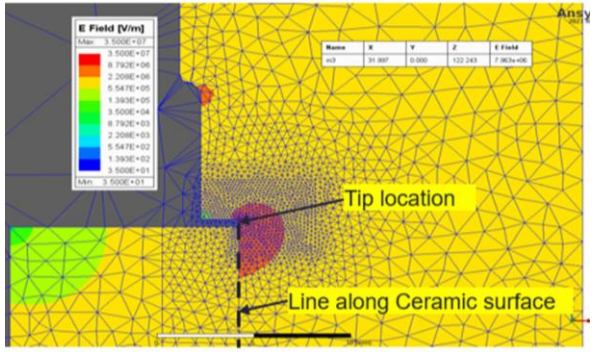
Source : Belau(Lam) et al. (2017), US Patent 10847374B2

The advancement to a 1000-layer NAND demands break through etch technologies. With scalable high-power solutions, unique pulsed plasma technology and Cryogenic etching, Lam is ideally positioned to lead the industry on this critical journey

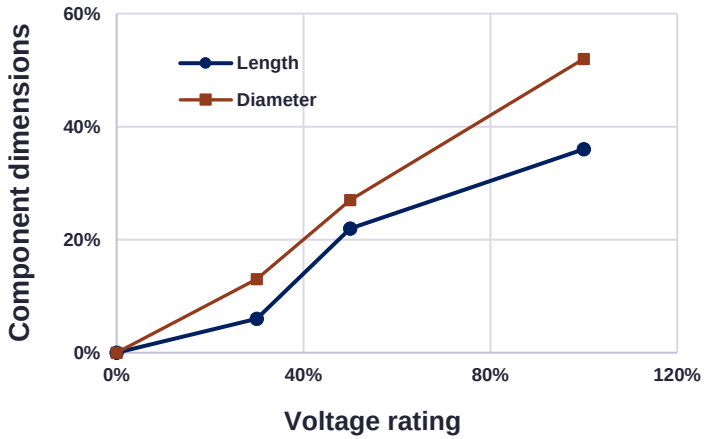
Challenges in RF Power Scaling for HAR Etching

Meeting the power scaling demands of 3D architectures places significant limitations on the RF design of critical power delivery subsystems.

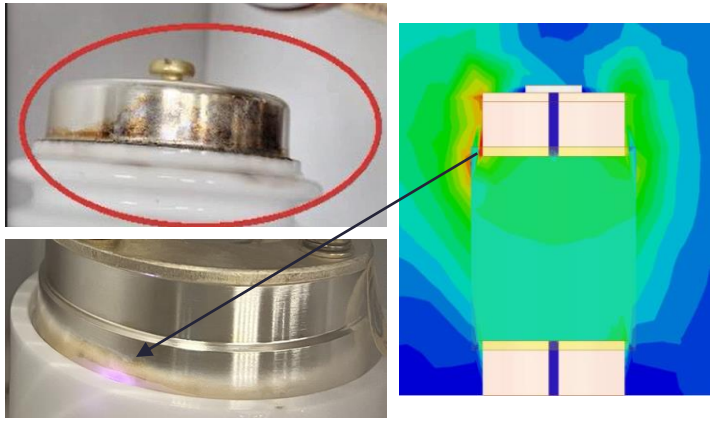
Creepage distance



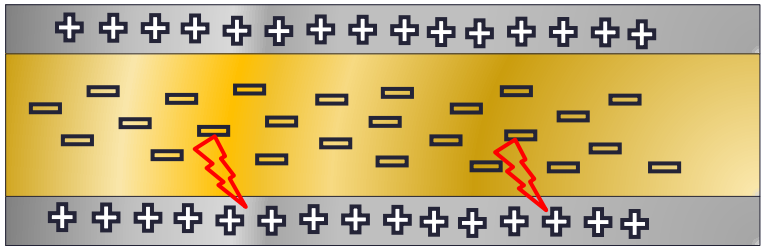
Component size



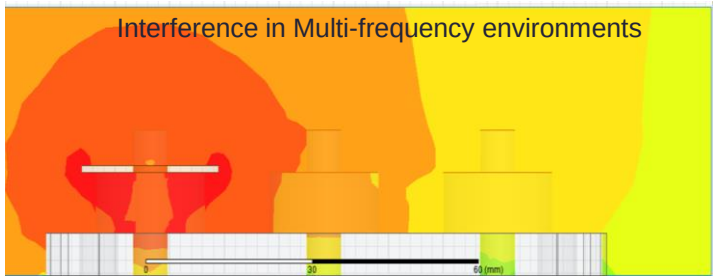
Arcing / Component Reliability



Cooling Solutions (Triboelectric effects)



EM Interference

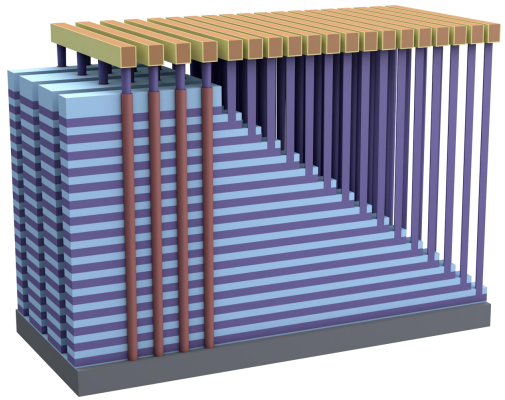


- Conventional RF power delivery designs are reaching their limits, demanding radical new architectures and component technologies for future scaling

Image Source : Lam INTERNAL

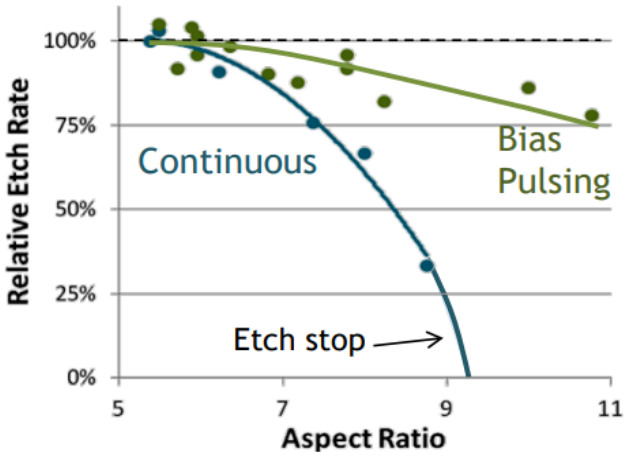
Achieving Profile Control in High Aspect Ratio Etch

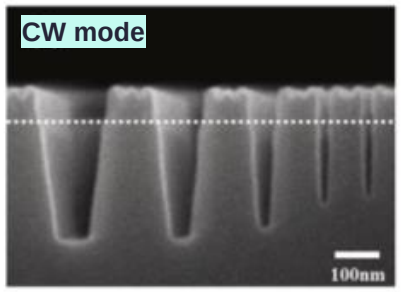
Maintaining consistent etch profiles and minimizing charging damage in 1000-layer 3D NAND will demand advanced pulsed RF techniques capable of delivering unprecedented precision in pulse shaping and timing control throughout the entire etch process.



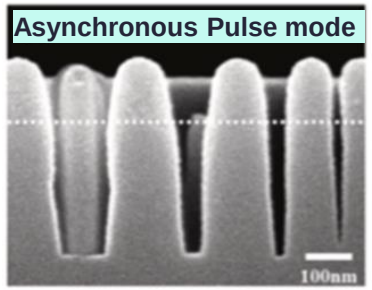
3D NAND
Aspect ratio > 40:1

Aspect Ratio Dependent Etching (ARDE)

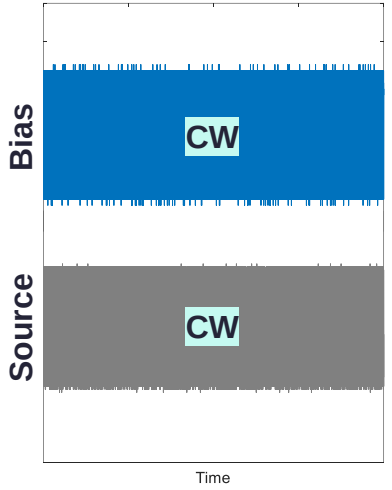


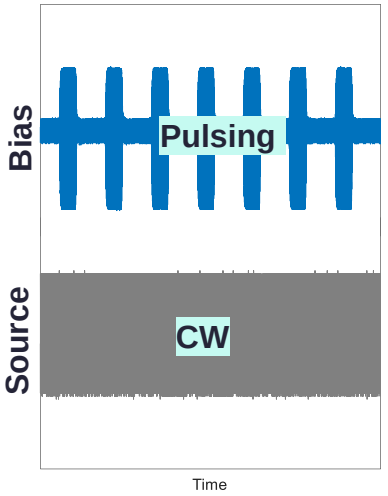


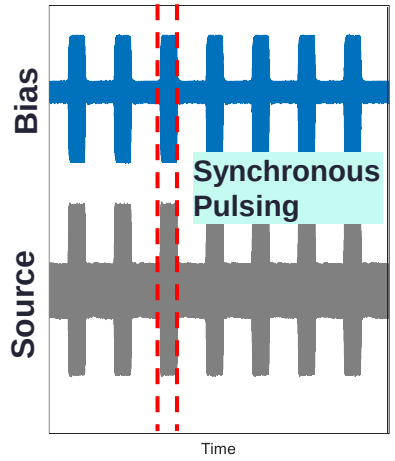
AR dependent (CW)



AR independent (Pulsing)







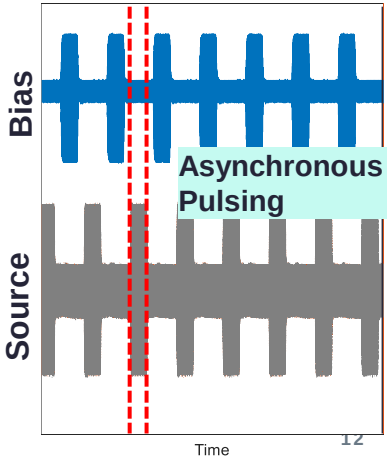
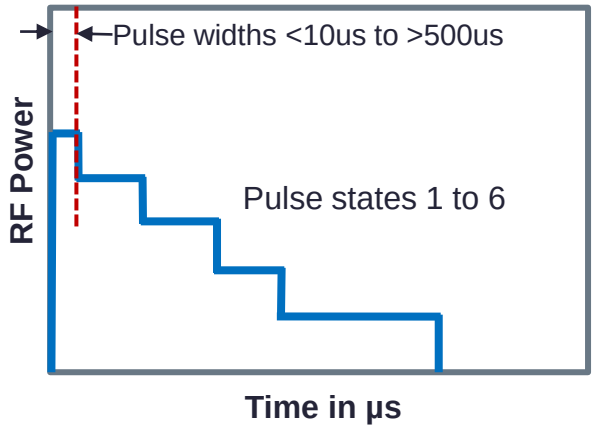


Image Source : Science Direct article, LAM Generated

Addressing Profile Control Challenges with Advanced Pulsing Schemes

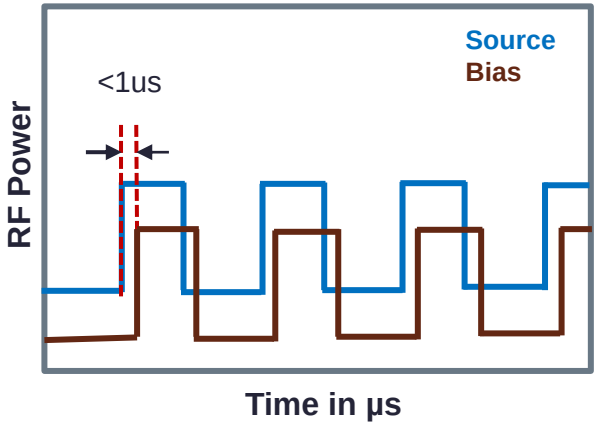
As semiconductor etching technology advances to meet the demands of smaller nodes, higher aspect ratios and stricter process control, RF pulsing techniques have become increasingly sophisticated

Multi-state Pulsing



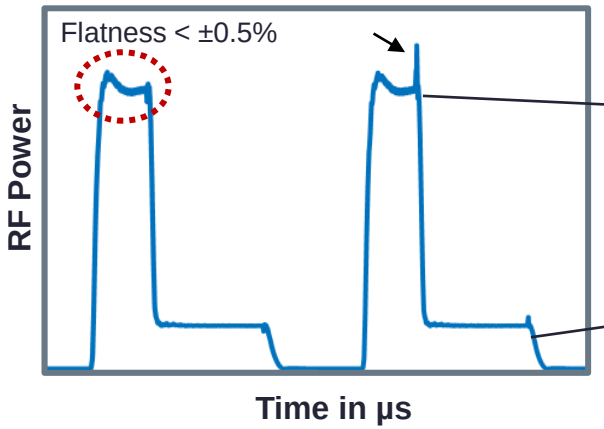
Complex waveform generation and control

Sub µs Timing control



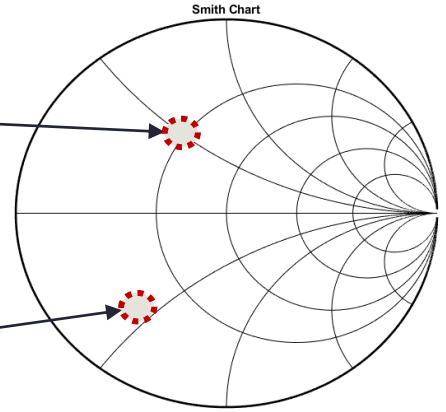
Sophisticated high- speed digital and analog control circuitry

Power stability



Advanced RF power amplifier design and feedback control loops

Impedance matching

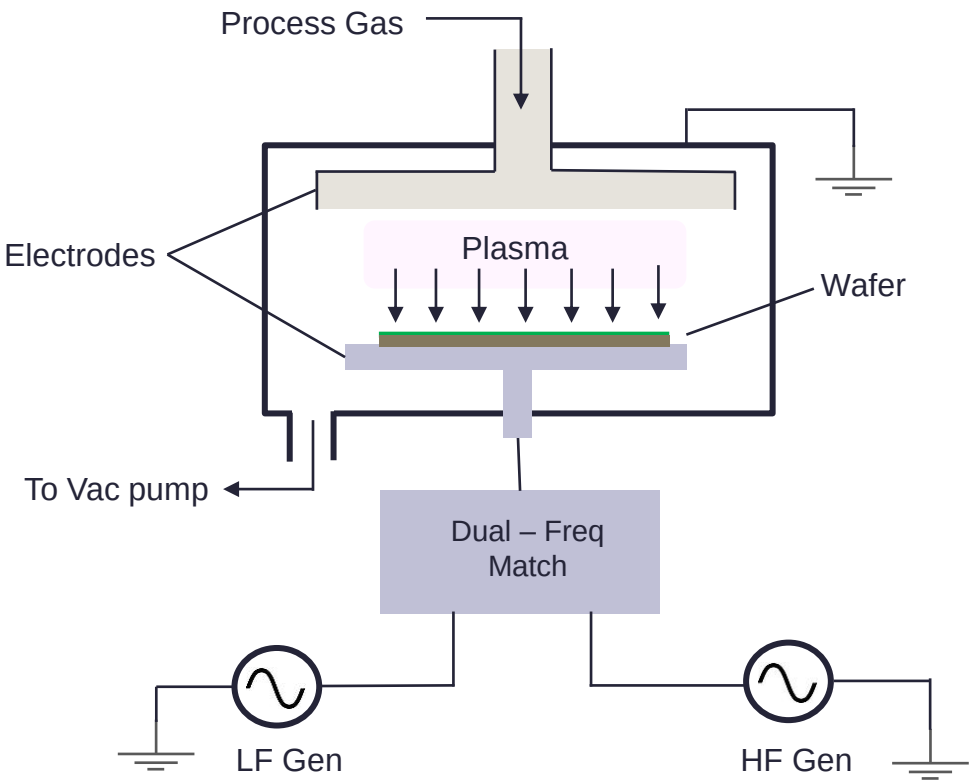


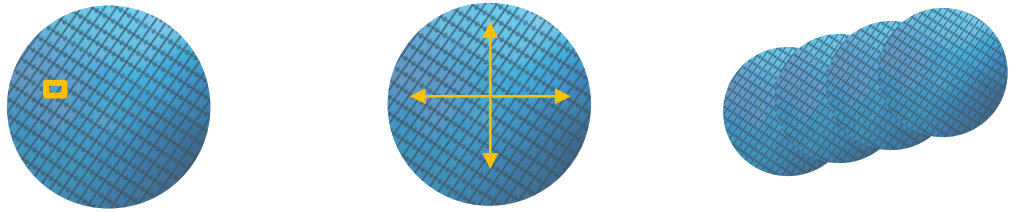
Ultra-fast and wide-band impedance matching networks

Source : Lam Generated

Uniformity & Repeatability Challenges in Advanced Etch

In advanced semi conductor etching, achieving exceptional uniformity and repeatability across the wafer is paramount to ensure consistent device performance and yield at nanoscale dimensions.





Within Die | Across Wafer | Volume production

Dual Frequency plasma systems provide critical tuning capabilities enabling a greater degree of control over ion energy and plasma density, essential for optimizing and maintaining uniformity

Key RF process variables in Dual-Frequency CCP Etch chambers :

RF Power
RF Frequency
Pulse Duty cycle
Pulse Frequency
Pulse Waveform
Match Network tune
Pulse timing /Synch
Phase difference

+

Chemistry
Gas Flow rates
Chamber Pressure
Wafer/Chamber temp
Electrode Gap

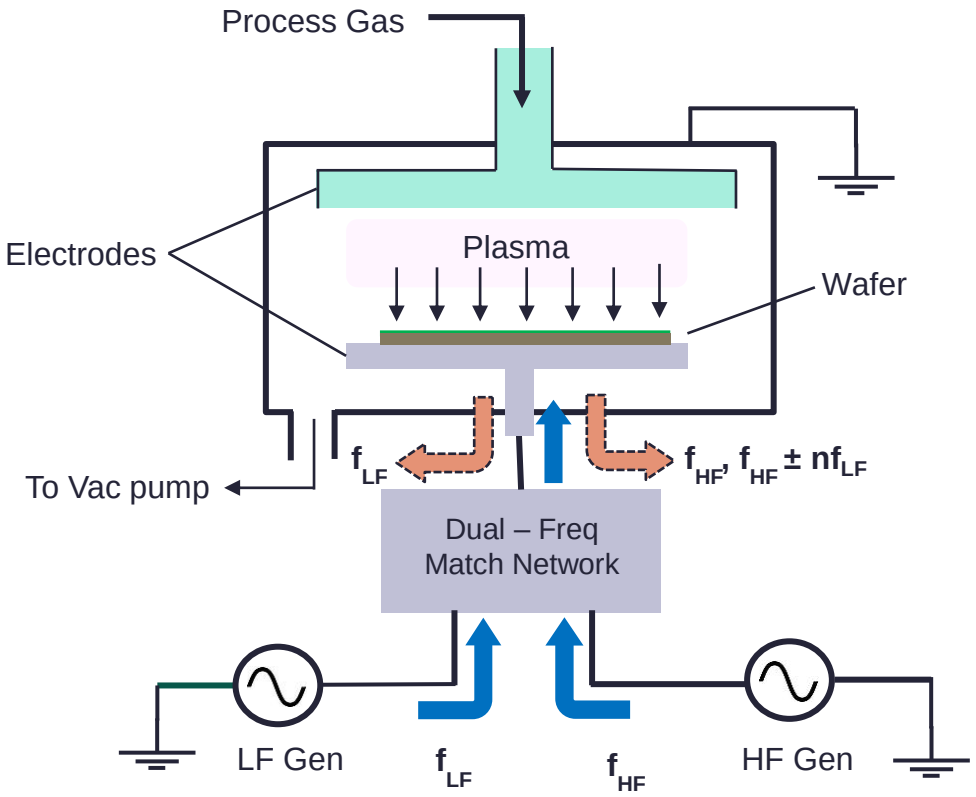
→

Etch rate
Etch Uniformity
Selectivity
Mask remain
CD Uniformity
Top CD
Bow CD

Source : Lam Generated

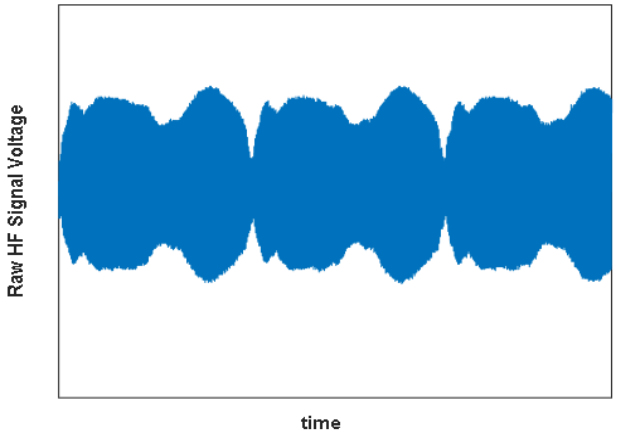
Challenges in Dual Frequency Plasma Systems

While dual-frequency plasma etch systems offer enhanced control over ion energy and plasma density, they also introduce unique challenges related to plasma non-linearities which can degrade efficiency and process performance

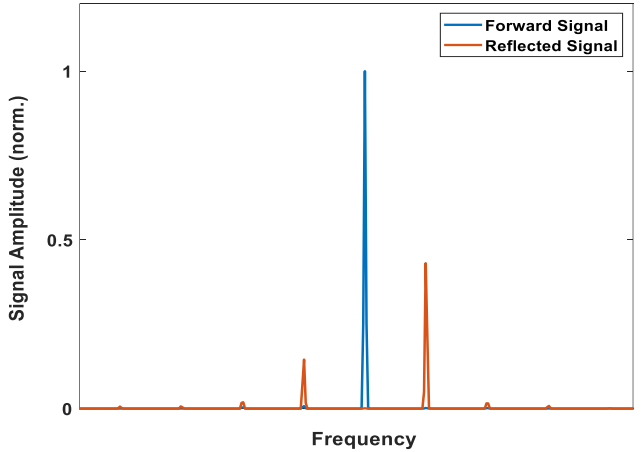


Unwanted frequencies generated due to non-linear mixing of input frequencies in dual frequency CCP plasma chambers can lead to :

- Etch Non-Uniformity
- Inefficient Power Delivery
- Thermal Overload
- Reduced process repeatability
- Narrower process window
- Increased risk of Hardware failure



Cross modulation due to Plasma sheath non-linearities



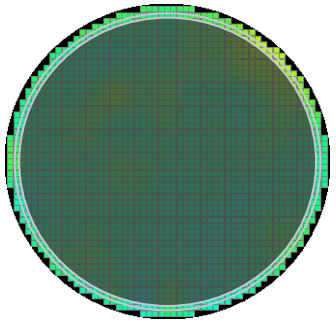
Unwanted frequency by products in Dual Freq CCPs

Sophisticated real-time feedback, powered by advanced sensing technologies is crucial to minimize the effects of these unwanted frequency components through dynamic frequency and power adjustment

Source : Lam Generated

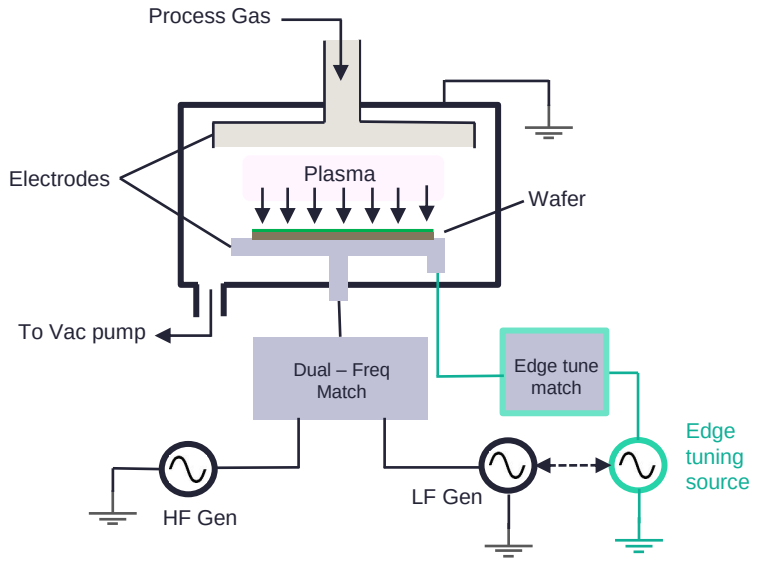
Wafer Edge Uniformity

Wafer edge uniformity is not just a technical challenge; it is a direct and significant driver of semiconductor manufacturing cost and profitability



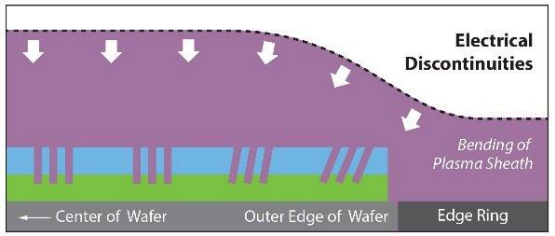
Outer 8 mm: ~10% of die

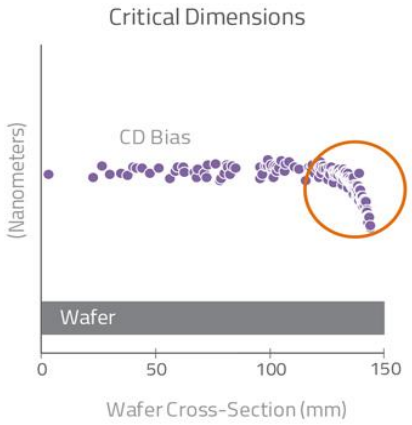
Outer 12 mm: ~20% of die

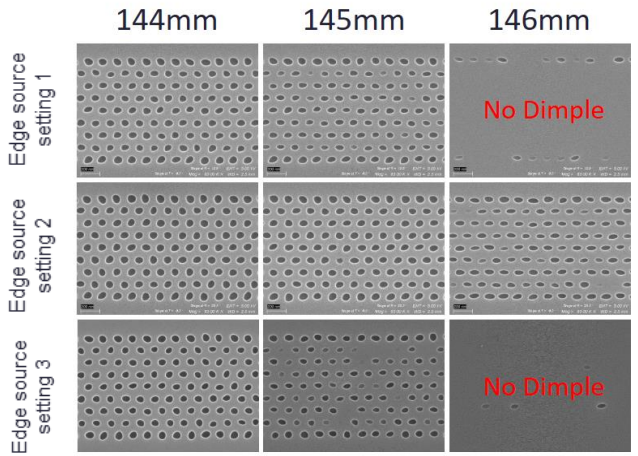


Edge non-uniformity and variability is primarily due to discontinuities at the edge

- Chemical discontinuity
- Thermal discontinuity
- Electrical discontinuity







HV CD-SEM Images of patterned wafers at three different edge source settings. Bottom dimple is observed only in setting 2 at 146mm

While a separate bias source can be employed for edge uniformity tuning, achieving truly independent control is very challenging due to the tight EM coupling at the wafer

Image Source : Semiconductor Engineering, semiconductor-digest, LAM Generated

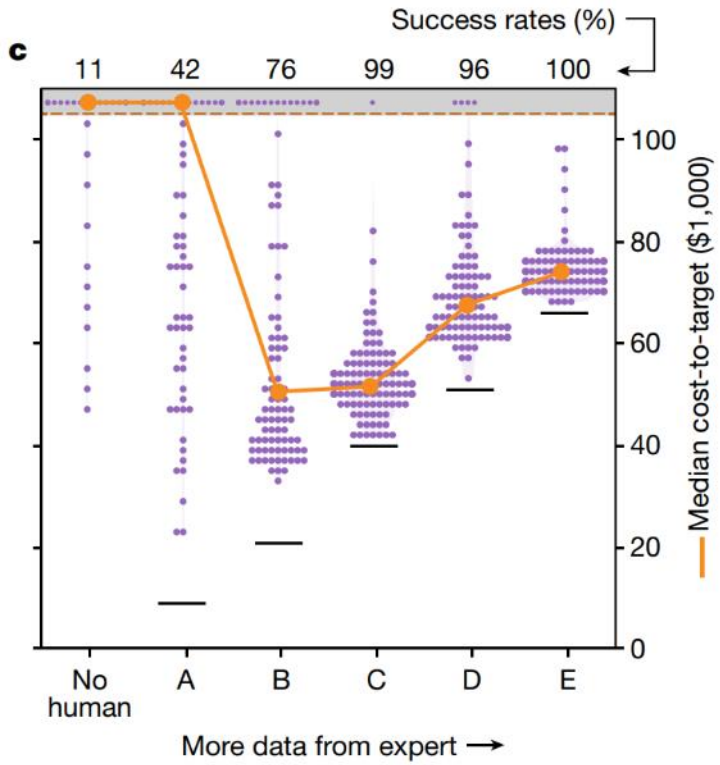
02

Speed-to-solution

Faster development by AI-assisted approach

AI-human collaboration is the key

Our paper suggests that the “human first-computer last” approach improves the development speed and cost (Karen et al., *Nature* **616** (2023) 707)



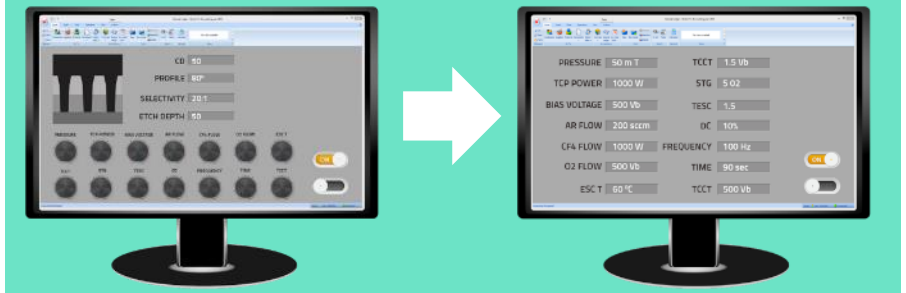
AI-assisted process development

Current approach (human only)

- Make hypothesis
- Design experiments
- Choose recipes
- Run experiments
- Perform metrology
- Data analysis

- $1000/recipe
- 1 day/ batch

Future (human + AI)

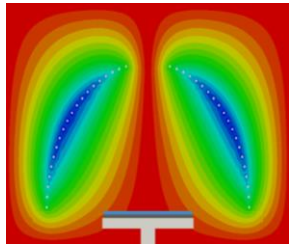


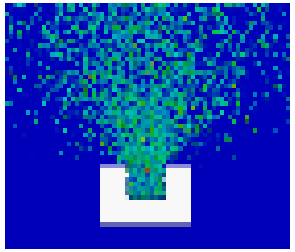
Plasma modeling: speed-to-solution at Lam

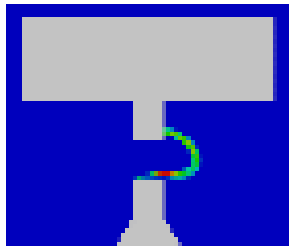
VizGlow™ as Lam in-house SW

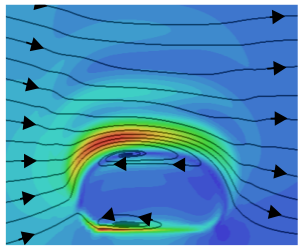
Lam acquired Esgee Technologies and VizGlow™ in 2022

Extensively used for modeling-driven HW design

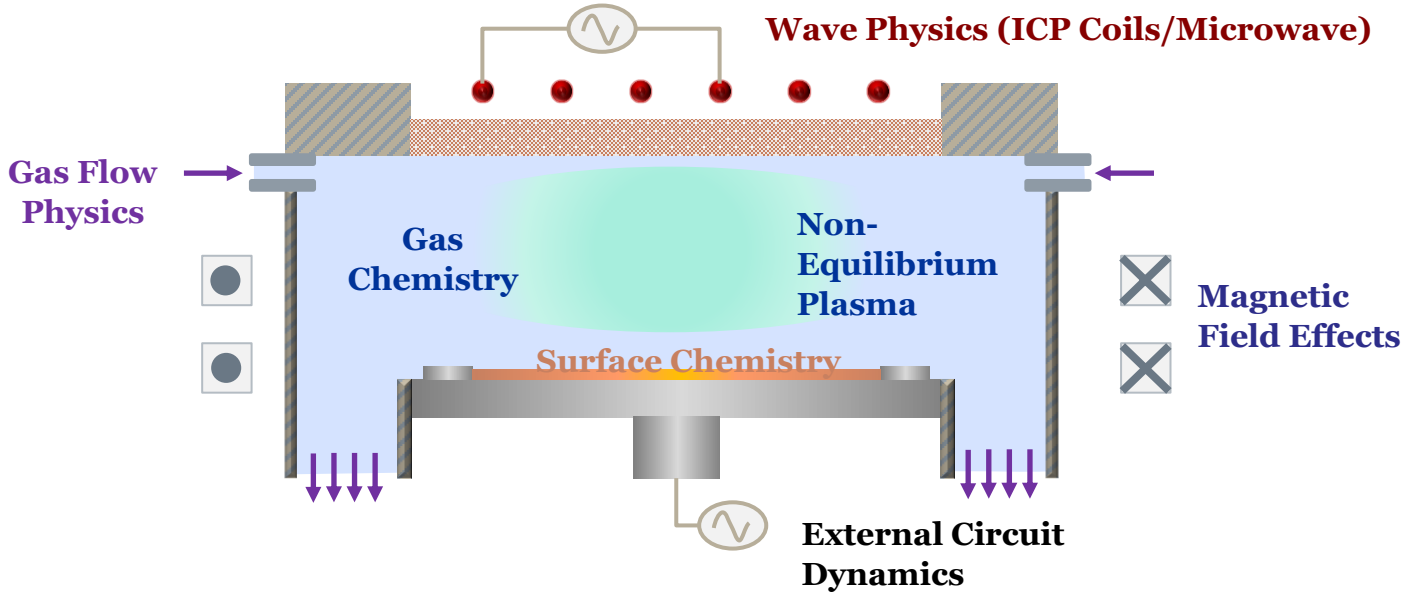








Overview



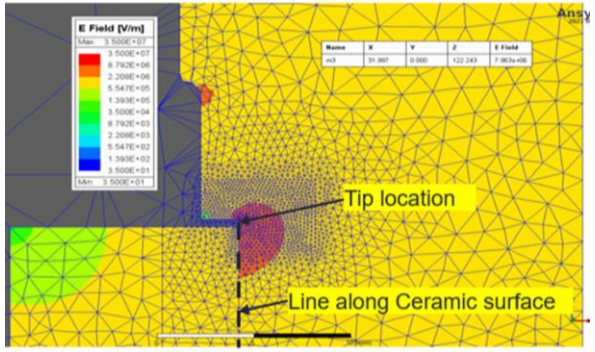
Discharge Types

- Capacitively Coupled Plasmas (CCP)
- Inductively Coupled Plasmas (ICP)
- Direct Current Plasmas (DC)
- Atmospheric Pressure Plasmas (APP)
- Microdischarges (MD)
- Microwave Plasmas (MWP)

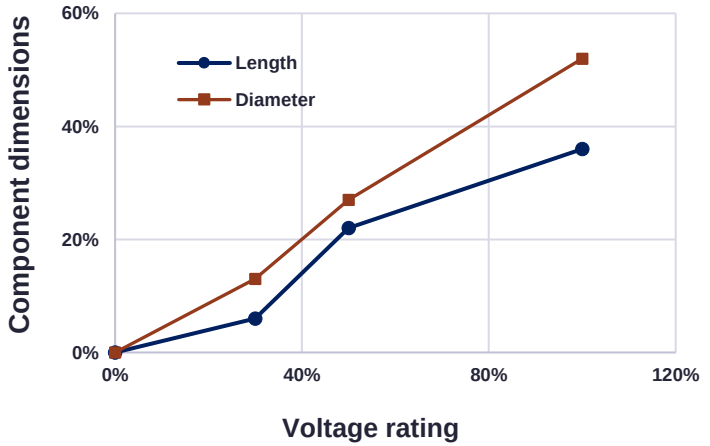
Modeling : Addressing the Challenges of Advanced Etch

Meeting the power scaling demands of 3D architectures places significant limitations on the RF design of critical power delivery subsystems.

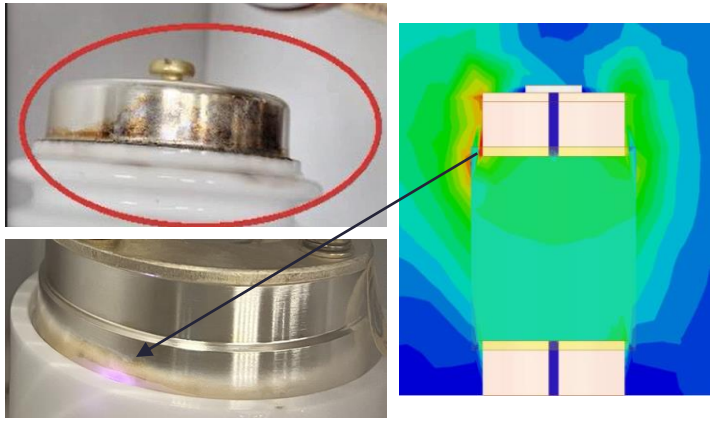
Creepage distance



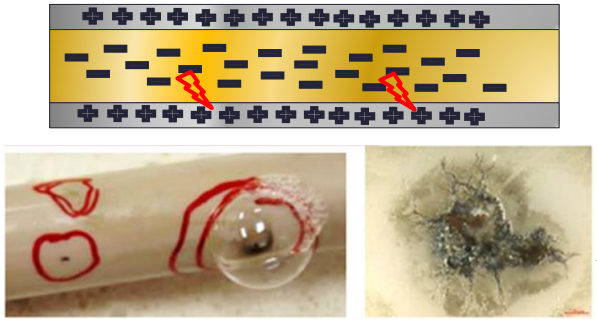
Component size



Arcing / Component Reliability



Cooling (Triboelectric effects)



- Advanced modeling and simulation tools are no longer optional; they are crucial for efficiently designing, optimizing and validating transformative technologies
- In semiconductor etch systems, the continuous flow of coolants through insulated lines can induce electrostatic charge build up resulting in arcing and damage to coolant lines.

EM Interference

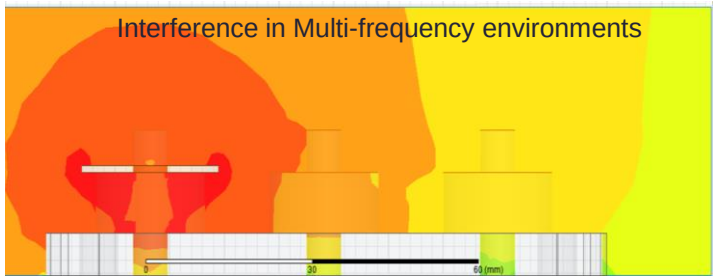
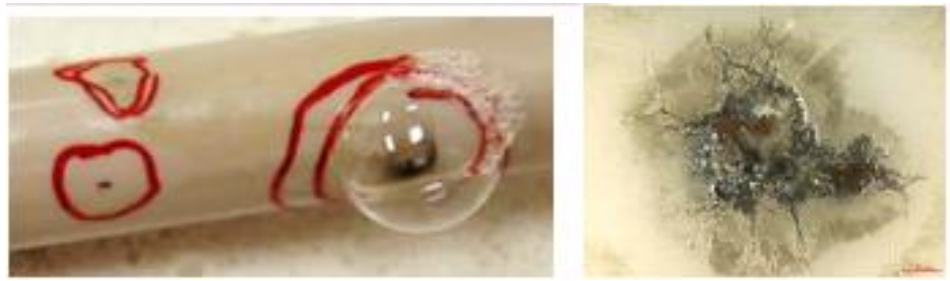


Image Source : Lam Generated

Modeling The Triboelectric Effect

Background

- Friction between dissimilar materials causes charge build-up
  - Nature of the coolant flowing through the tubing generates charge buildup
- This charge build-up over time causes arcing



Damaged coolant lines

Research in other industries

- Petro-chemical, consumer electronics
- Flow of gasoline through pipes caused arcing and resulted in catastrophic explosions
  - Research to prevent such scenarios resulted in developing models

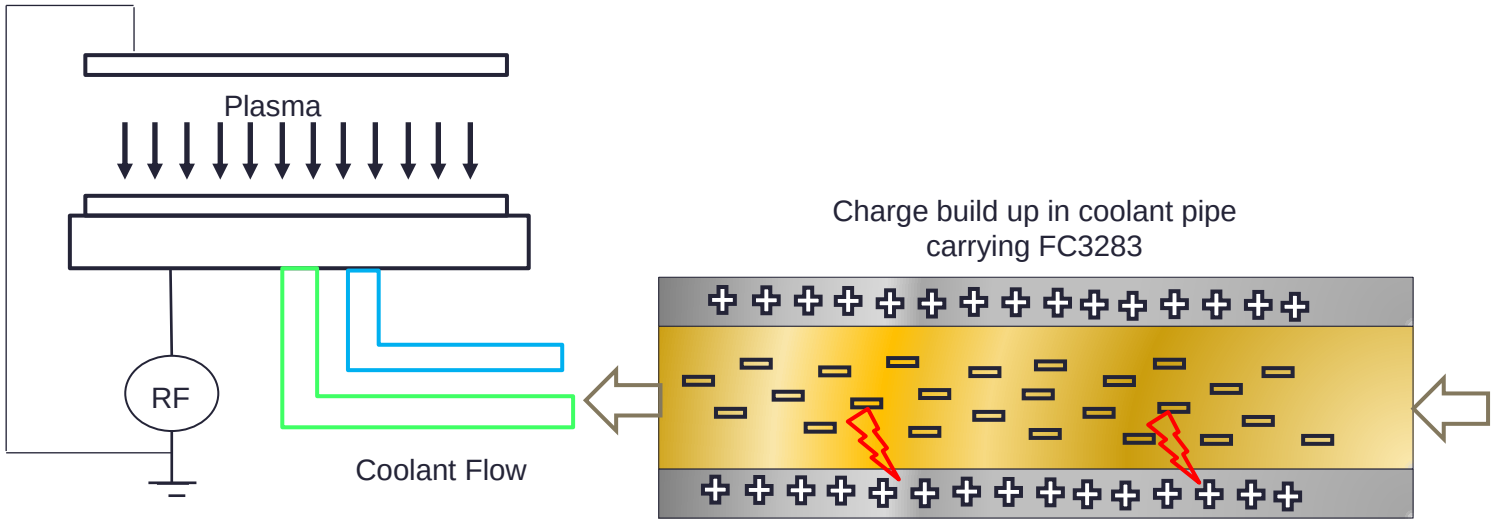


Image Source : Lam Generated

Turbulent Kinematic Viscosity (Dt) captures eddy action

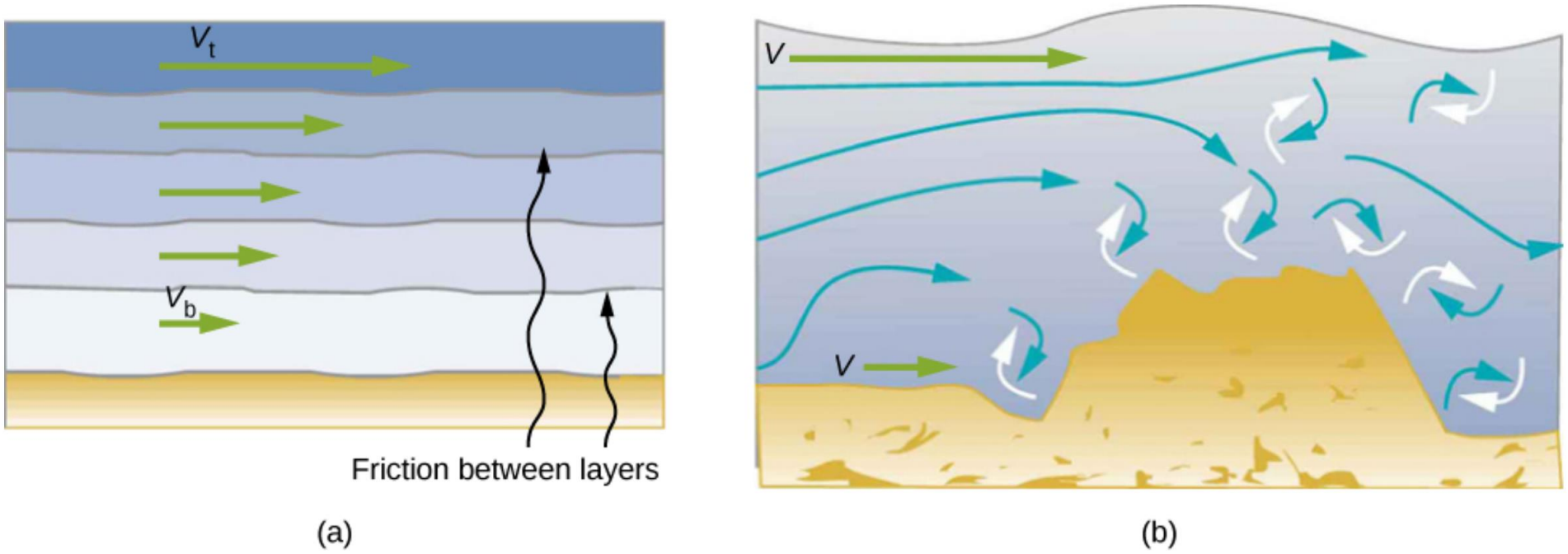


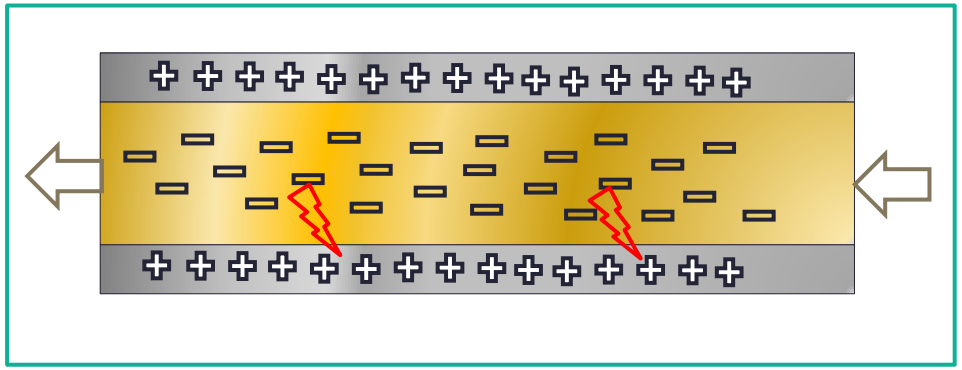
Figure 14.34 (a) Laminar flow occurs in layers without mixing. Notice that viscosity causes drag between layers as well as with the fixed surface. The speed near the bottom of the flow (v_b) is less than speed near the top (v_t) because in this case, the surface of the containing vessel is at the bottom. (b) An obstruction in the vessel causes turbulent flow. Turbulent flow mixes the fluid. There is more interaction, greater heating, and more resistance than in laminar flow.

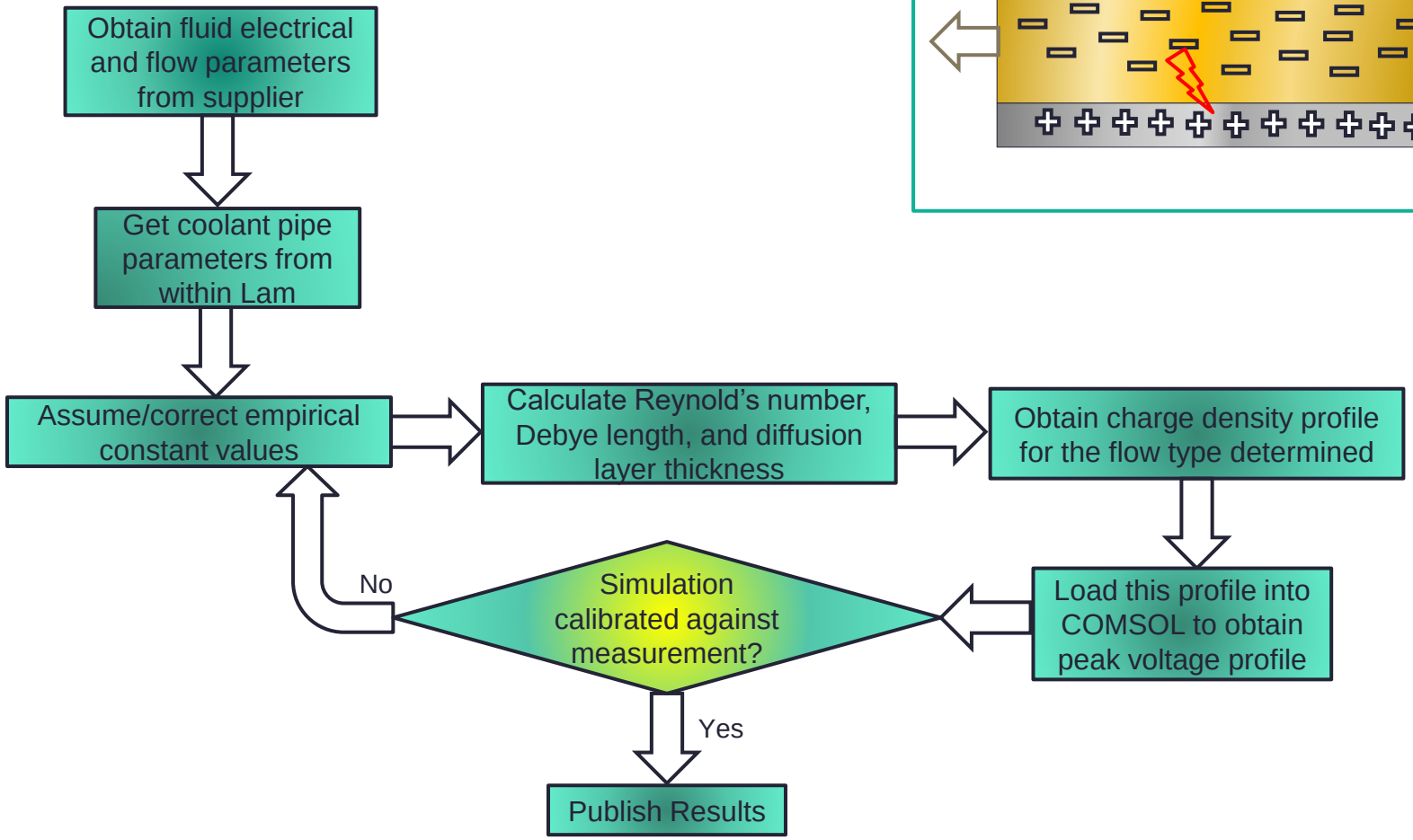
Friction not only exists between fluid and pipe but also between internal layers of the fluid itself

https://courses.lumenlearning.com/suny-osuniversityphysics/chapter/14-7-viscosity-and-turbulence/

Tribo-electric Model Overview

Flow Chart to model the physics of flow electrification





Flow chart details with equations

1) Get the following parameters of the coolant from supplier

- Relative permittivity (ε_r) , Electrical conductivity (σ), Kinematic Viscosity (ν), Density of fluid (ρ)

2) Obtain the following coolant pipe information from within Lam

- Pipe radius (a) , Pipe length ($L1$), Velocity of fluid flow (Um), Temperature of fluid flow (T)

3) Derive empirical constants using experiment and modeling

- initially assume values – come back and correct
- m, k, n, $At2$, and Diffusion coefficient (D) which is dependent on Temperature and velocity of fluid flow

4) Calculate the following parameters to determine flow type

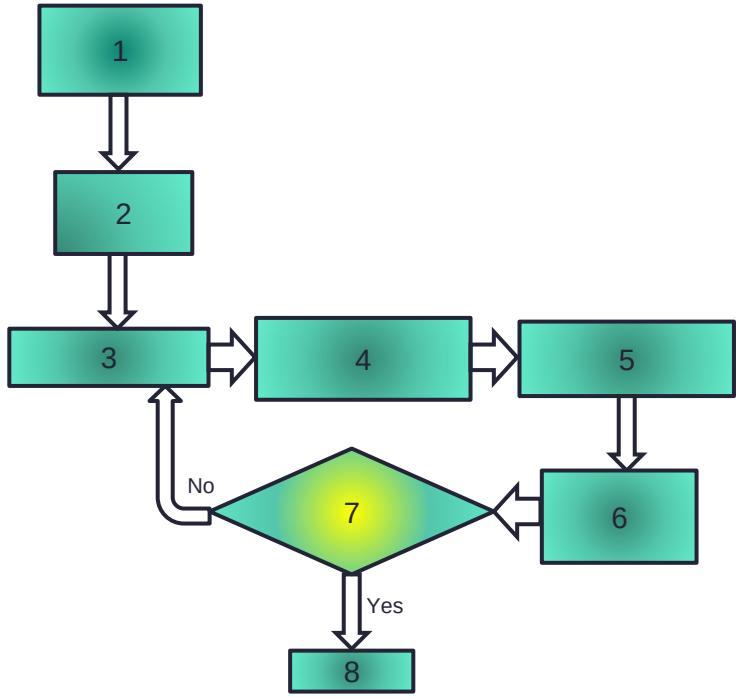
- Reynold's number $Re = \frac{2aUm}{\nu}$
  - If Re >3500 flow is turbulent otherwise it is laminar flow
- Schmitt's number $S = \frac{\nu}{D}$
  - Which gives diffusion sublayer thickness δ
- Debye length $\lambda = \left(\frac{D\varepsilon_o\varepsilon_r}{\sigma}\right)^{\frac{1}{2}}$

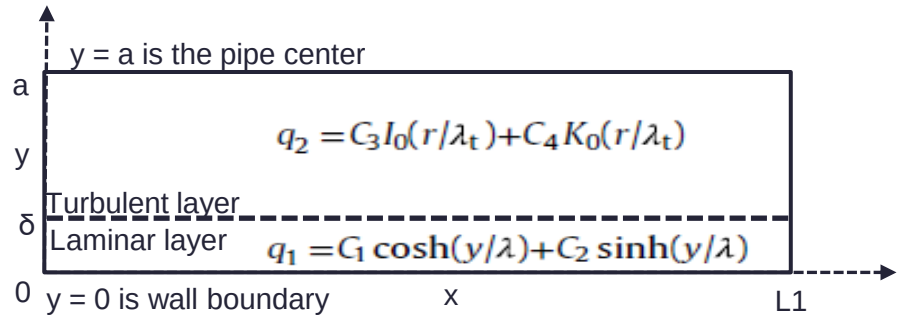
5) Obtain charge density distribution for the flow type determined [1]

6) Load charge density into Poisson's to get Voltage, E-fields

$\nabla \cdot \mathbf{D} = \rho_v$ = q1, q2

7) Simulation vs Measurement calibration





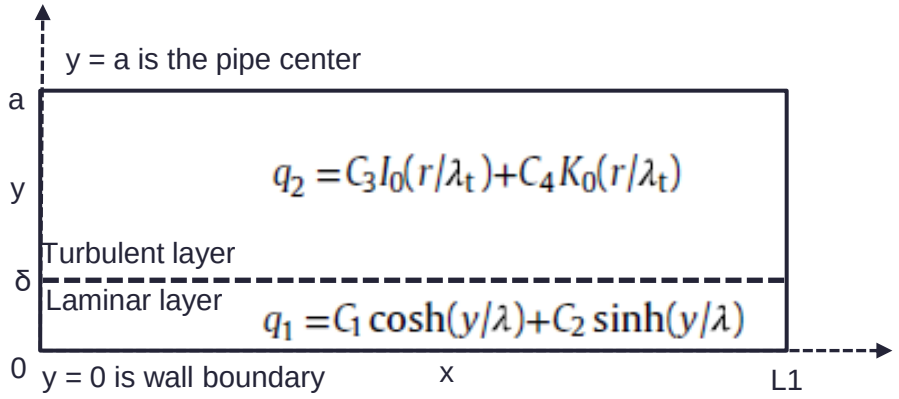
[1]Xu Diao, Juncheng Jiang, Lei Ni, Ahmed Mebarki, Guodong Shen, Electrification hazard of turbulent pipe flow: Theoretical approach and numerical simulation, Process Safety and Environmental Protection, Volume 159, 2022, Pages 84-95

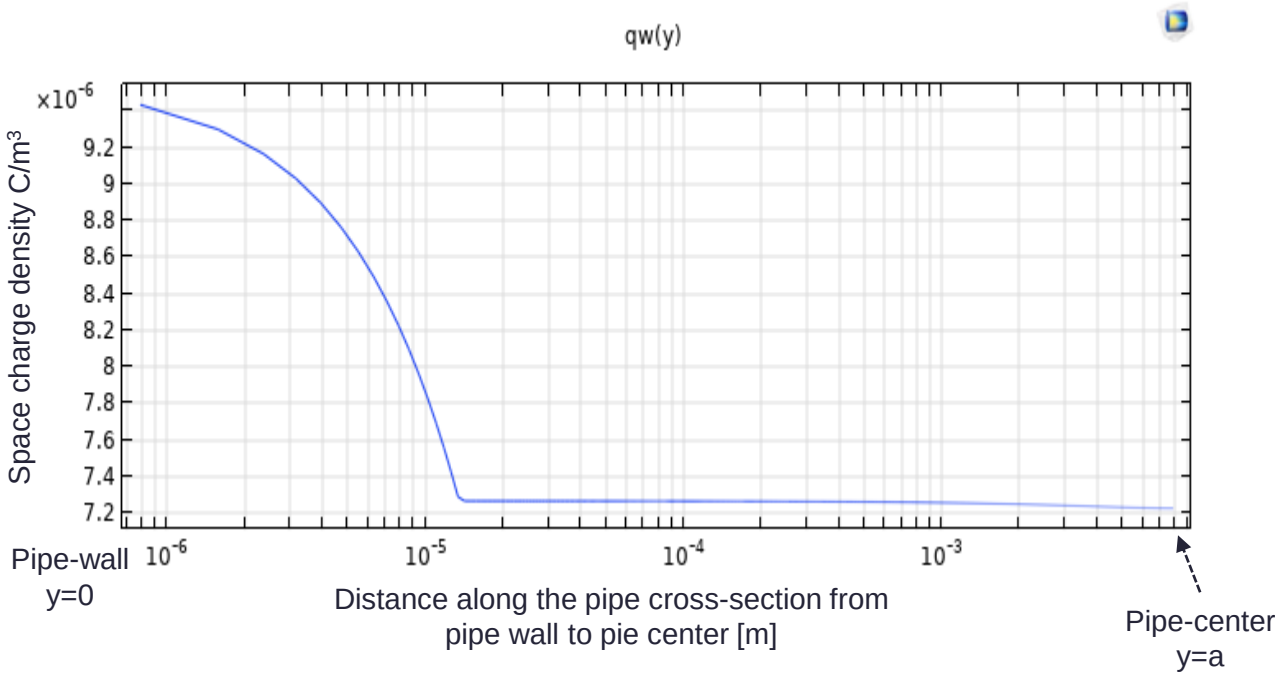
Fluid dynamic parameters for FC3283

Parameters	Fluorinert FC-3283
Radius of pipe, a [m]	0.00787
Length of pipe, L1 [m]	0.6096
Average Velocity, Um [m/s]	1.45
Density, ρ [kg/m^3]	1820
Relative permittivity, ε_r	1.89
Conductivity of fluid, σ [S/m]	1e-13
Molecular diffusion coefficient, Dm [m^2/s]	1e-9
Kinematic viscosity, v [m^2/s]	0.75e-6

Derived Parameters	Fluorinert FC-3283
Reynold's number : Re	30,431
Schmitt's number	750
Diffusion sub-layer thickness: δ [m]	1.35e-5
Debye Length: λ [m]	4.1e-4

- Our fluid parameters indicate turbulent regime since Re>3500 and the flow region should have both laminar and turbulent layers
- This space charge density profile is applied along the entire length of the pipe in COMSOL electrostatics module





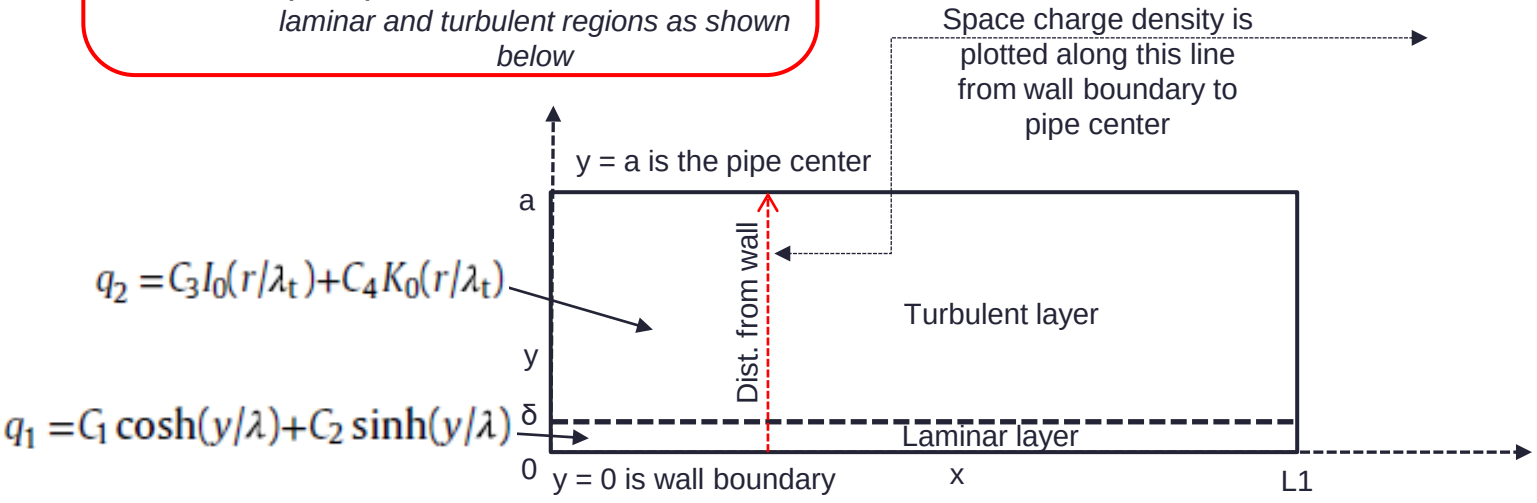
[1]Xu Diao, Juncheng Jiang, Lei Ni, Ahmed Mebarki, Guodong Shen, Electrification hazard of turbulent pipe flow: Theoretical approach and numerical simulation, Process Safety and Environmental Protection, Volume 159, 2022, Pages 84-95

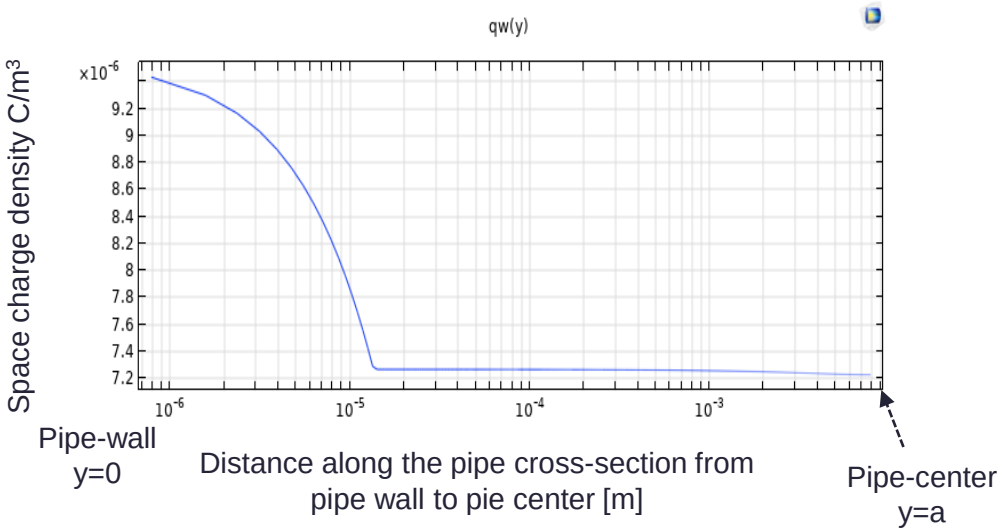
Poisson Equation to get voltage distribution in COMSOL

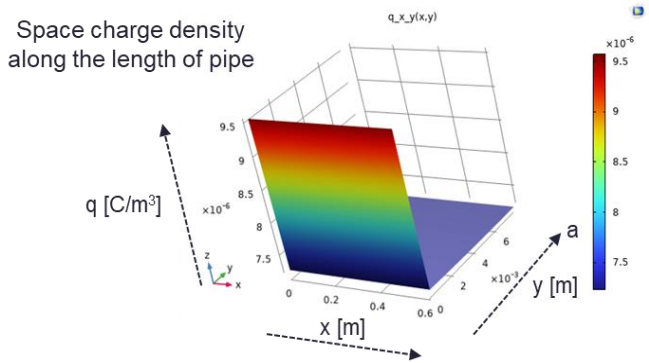
Stationary Study

$$\mathbf{E} = -\nabla V$$
$$\nabla \cdot (\epsilon_0 \epsilon_r \mathbf{E}) = \rho_v$$
$$\nabla^2 V = -\frac{\rho}{\epsilon_0}$$

$\rho = q$ *which is defined separately for laminar and turbulent regions as shown below*



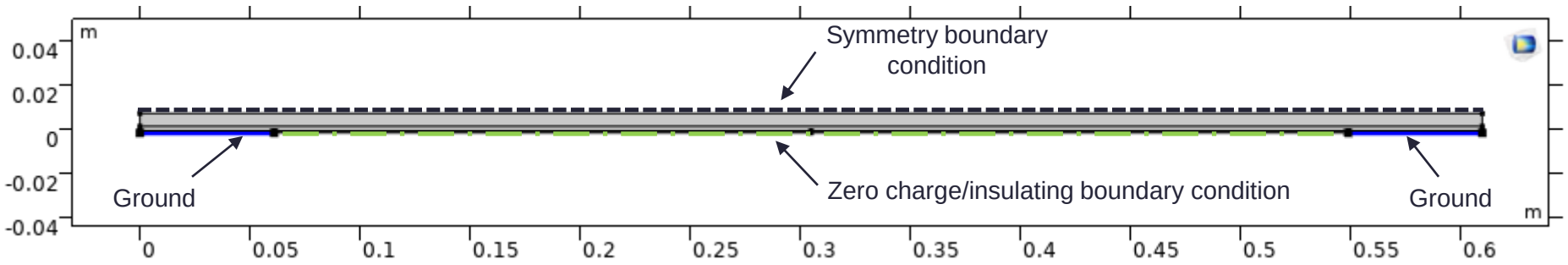




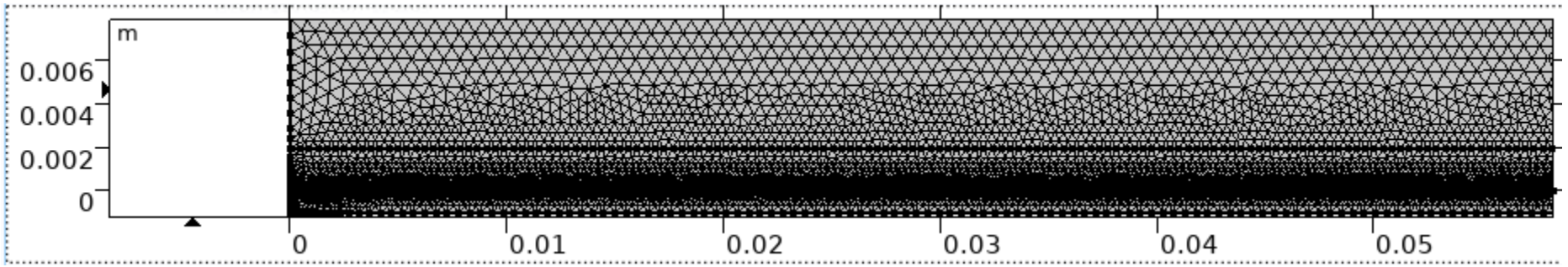
Fluid dynamics and electrostatic equations are combined to determine the tribo-electric effect of coolant pipes

[1]Xu Diao, Juncheng Jiang, Lei Ni, Ahmed Mebarki, Guodong Shen, Electrification hazard of turbulent pipe flow: Theoretical approach and numerical simulation, Process Safety and Environmental Protection, Volume 159, 2022, Pages 84-95

Boundary Conditions and Meshing in COMSOL model

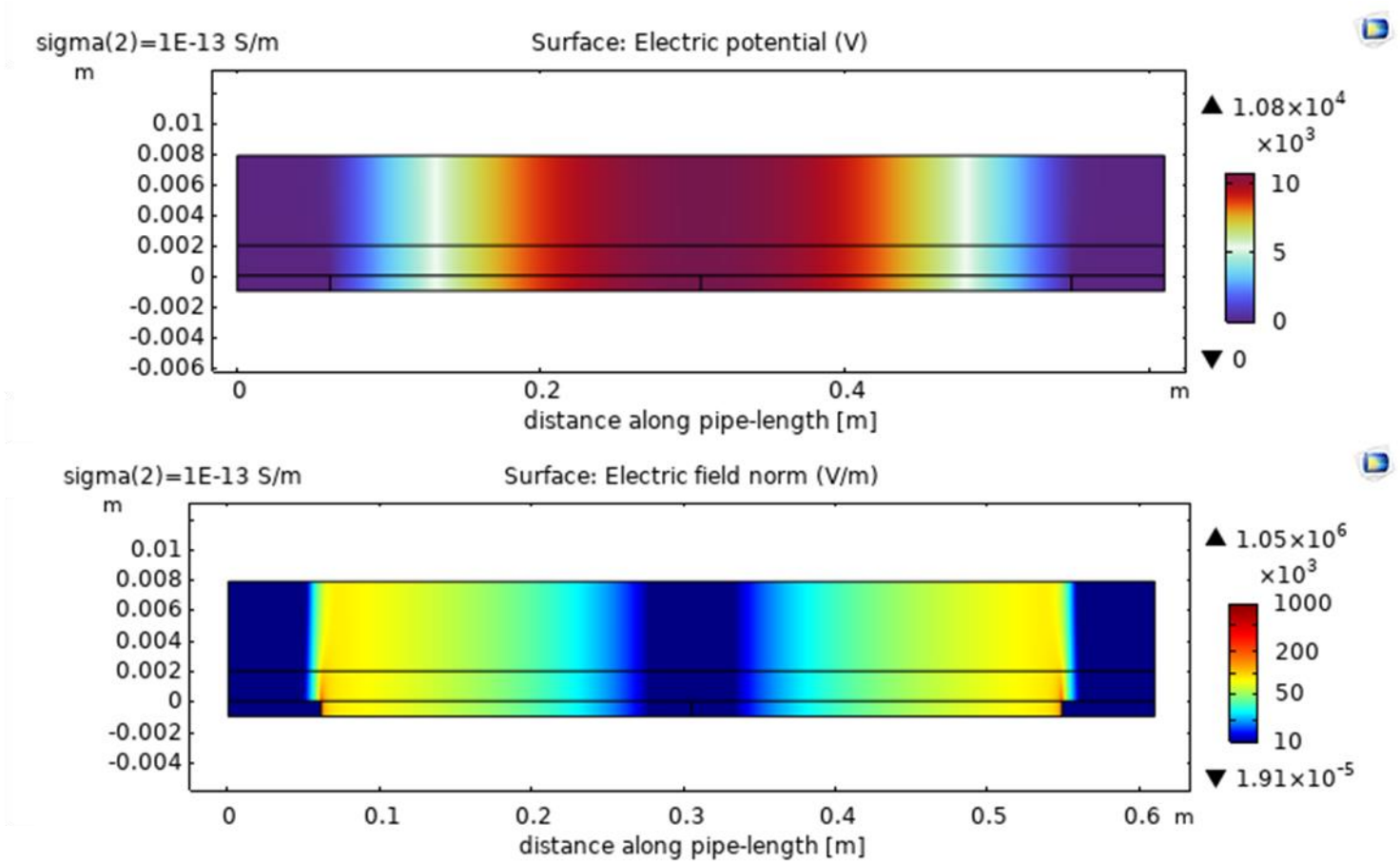


Boundary conditions applied in COMSOL model



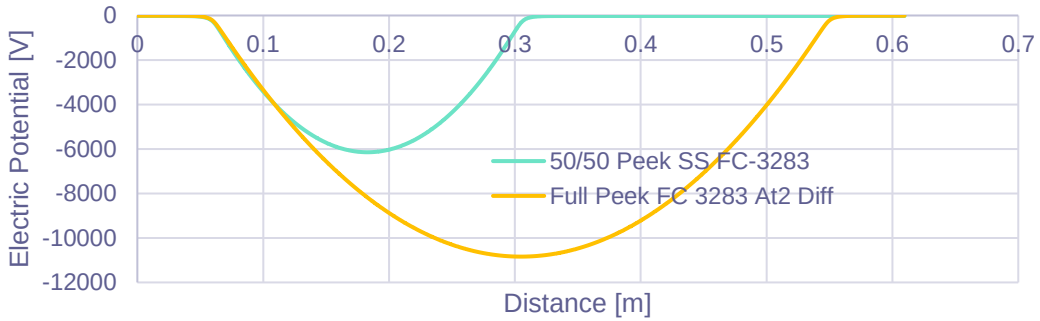
Diffusion layer near the wall is very narrow, and for accurate representation of the fluid dynamics within this layer, mesh element should be of the order of Debye Length

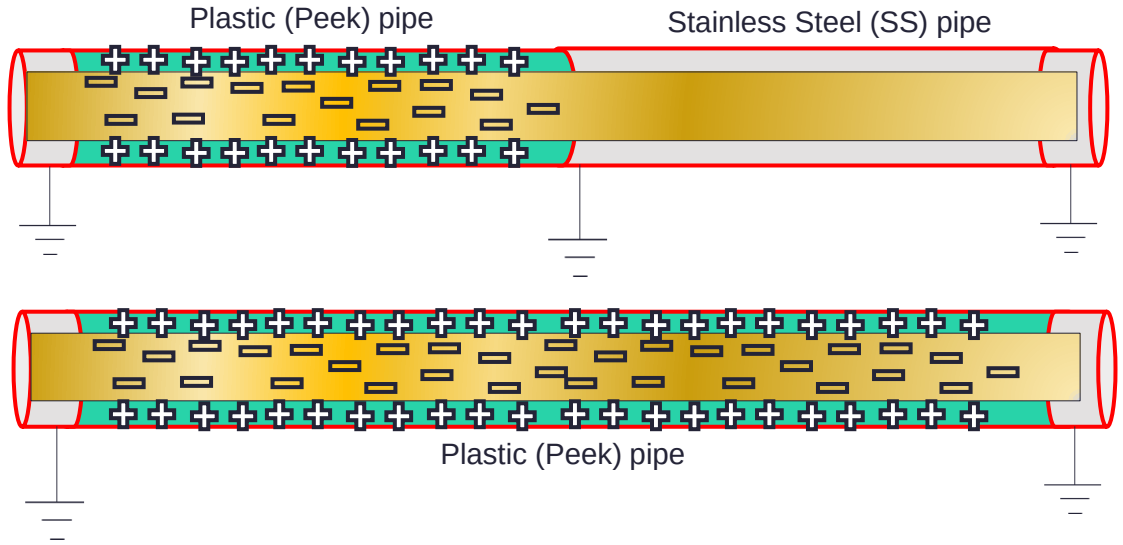
Results in COMSOL model



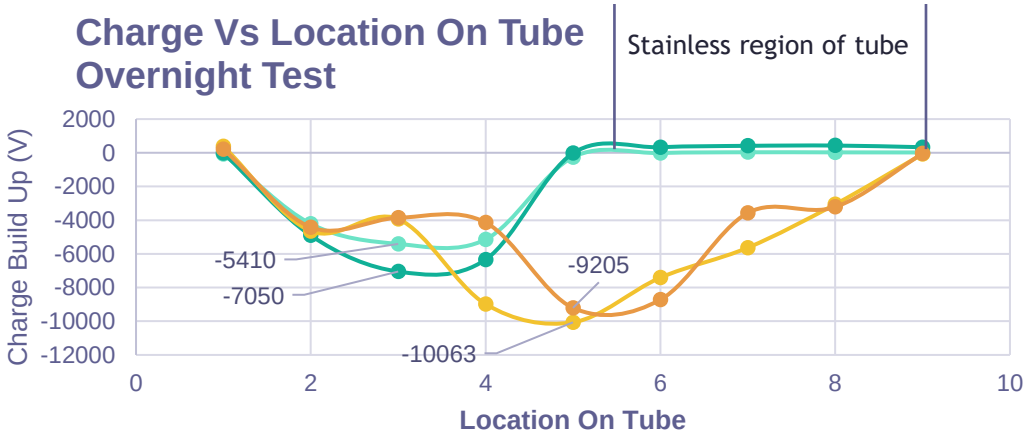
Max voltage is at the center of the tube and Max E-field is between the grounded stainless-steel part and the dielectric tube

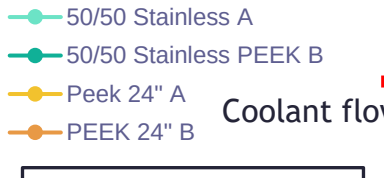
Simulation vs Measurement



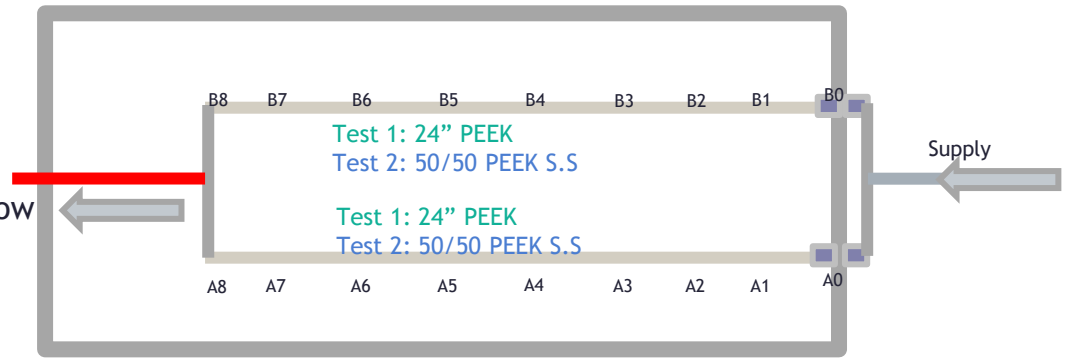


Simulation





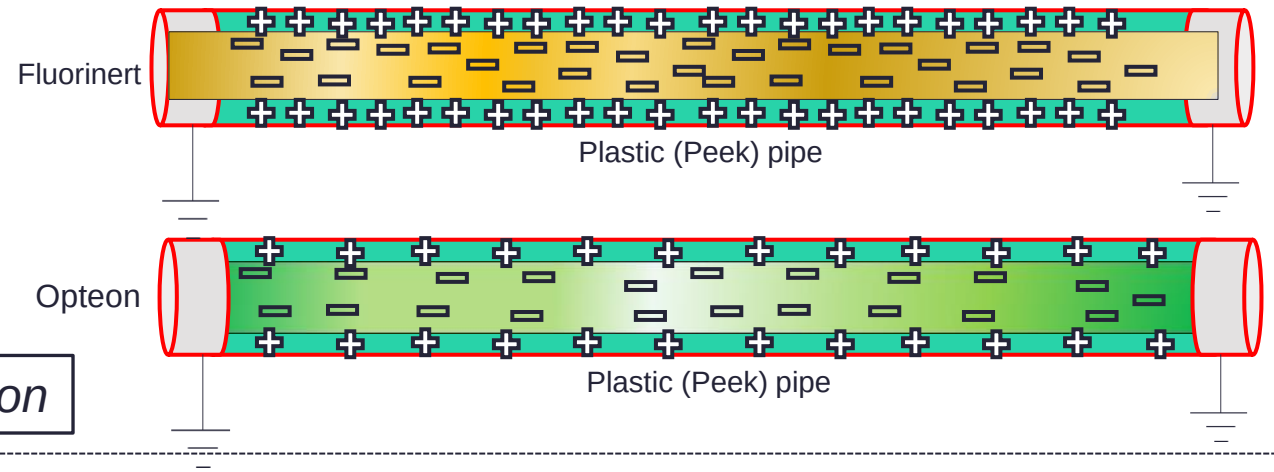
Measurement



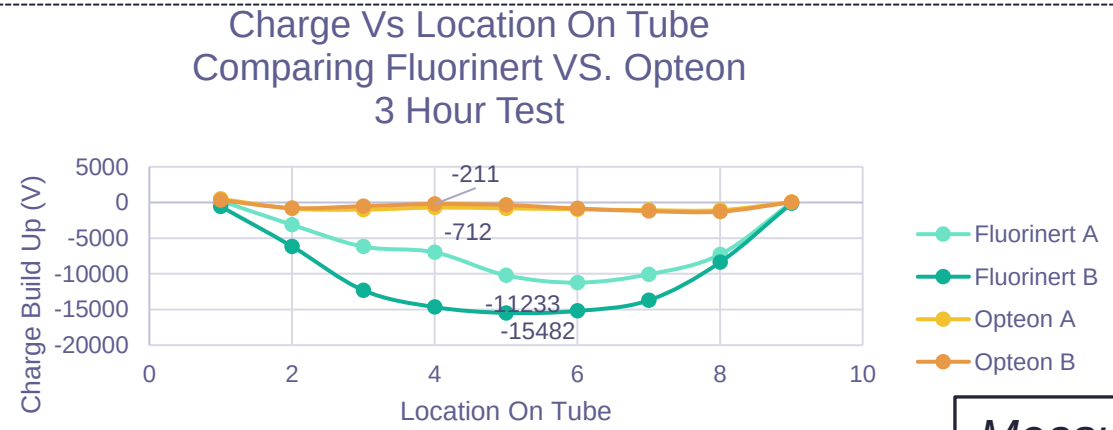
Grounded coolant pipe neutralizes charges and decreases risk of Tribo-Electric discharge

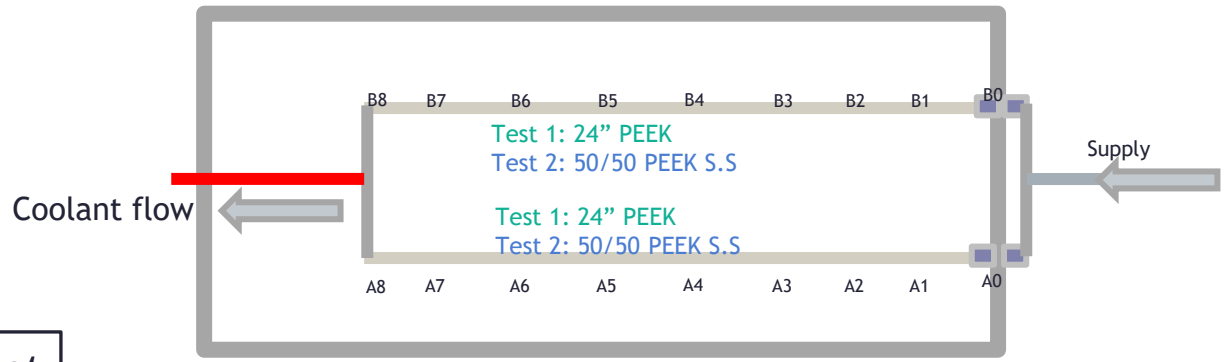
Coolant Change: Simulation vs Measurement

Parameters	Fluorinert FC 3283	Opteon SF 10
Conductivity of fluid, σ [S/m]	1e-13	4.54e-10



Simulation

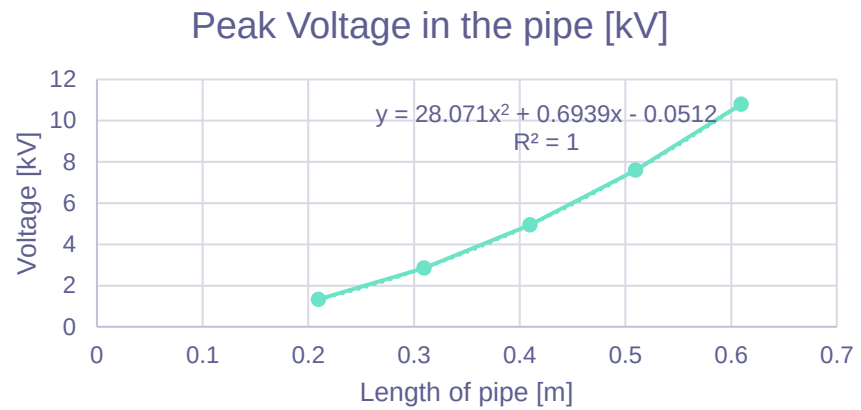


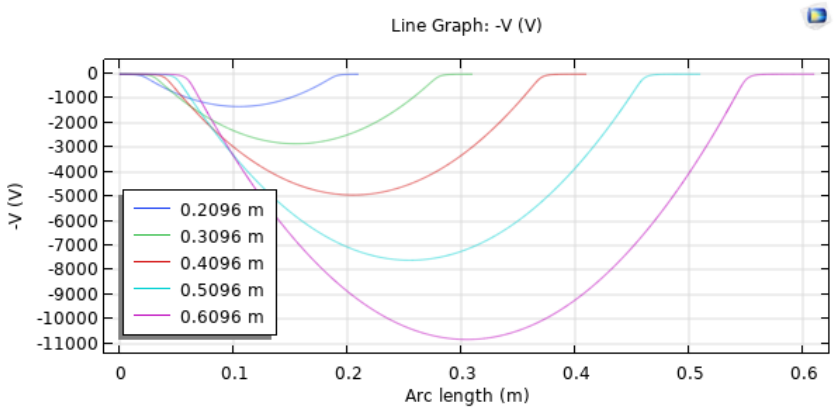


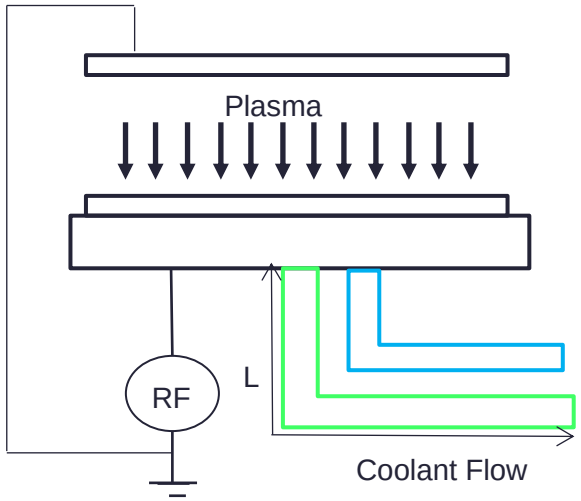
Measurement

Coolant with higher electrical conductivity poses less risk in Tribo-electric discharge since there are enough charge carriers to neutralize the arc risk

Peak Voltage Dependence on Length of Pipe



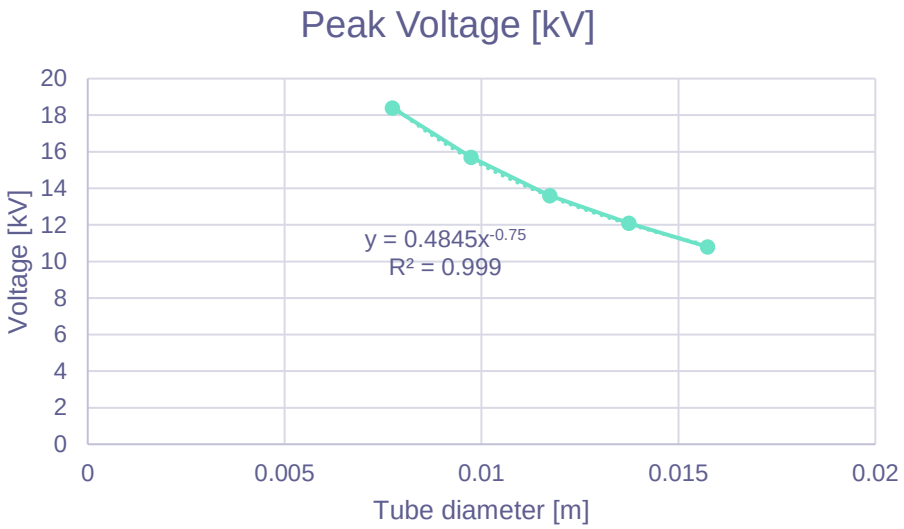


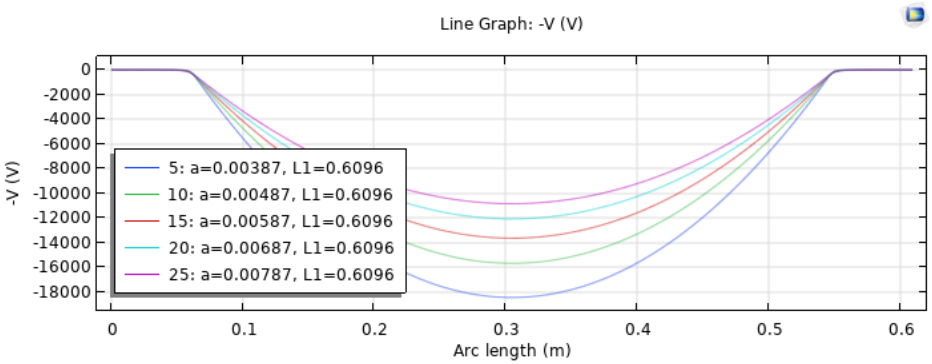


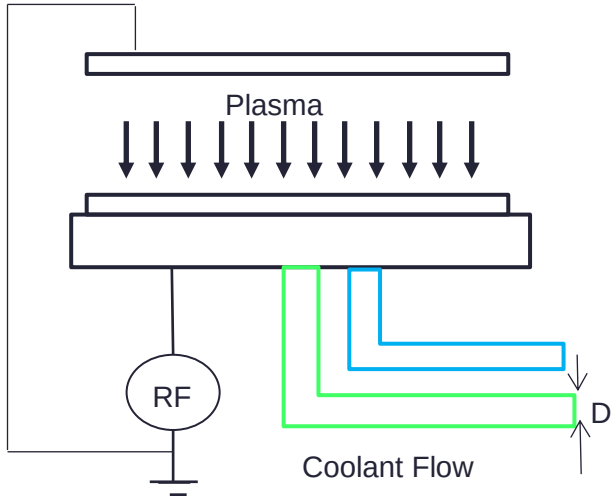
Peak voltage is directly proportional to the length of pipe and results reasonably agree with [3]

[3] Varga, I.K., 1980. The tribo-electric effect of liquid flow and its applications.

Peak Voltage Dependence on Diameter of Pipe





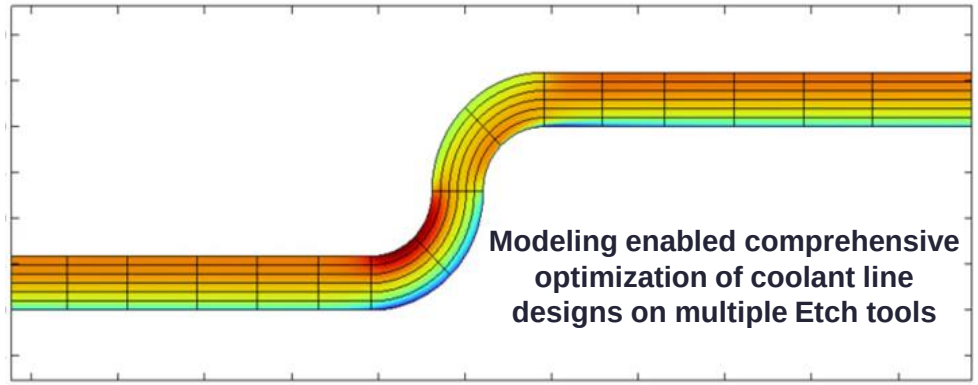


Peak voltage is inversely proportional to the tube diameter and results reasonably agree with [3]

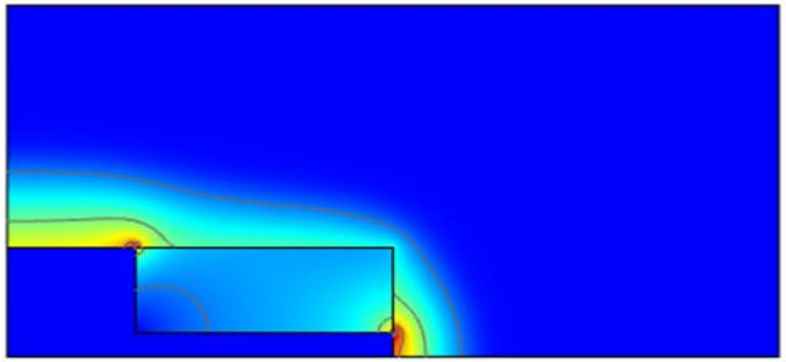
[3] Varga, I.K., 1980. The tribo-electric effect of liquid flow and its applications.

Model Based Solutions to RF related problems

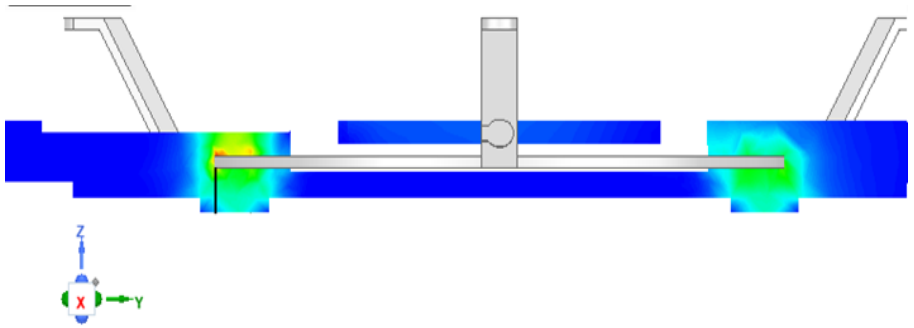
Coolant Pipe Design Improvement



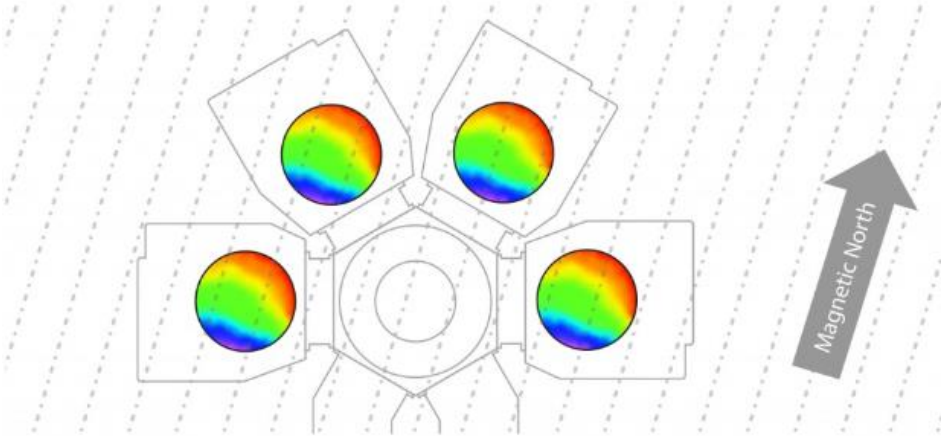
Extreme Edge Uniformity Improvement



Design margin Verification for High Voltage



Magnetic Shielding solutions to improve chamber matching

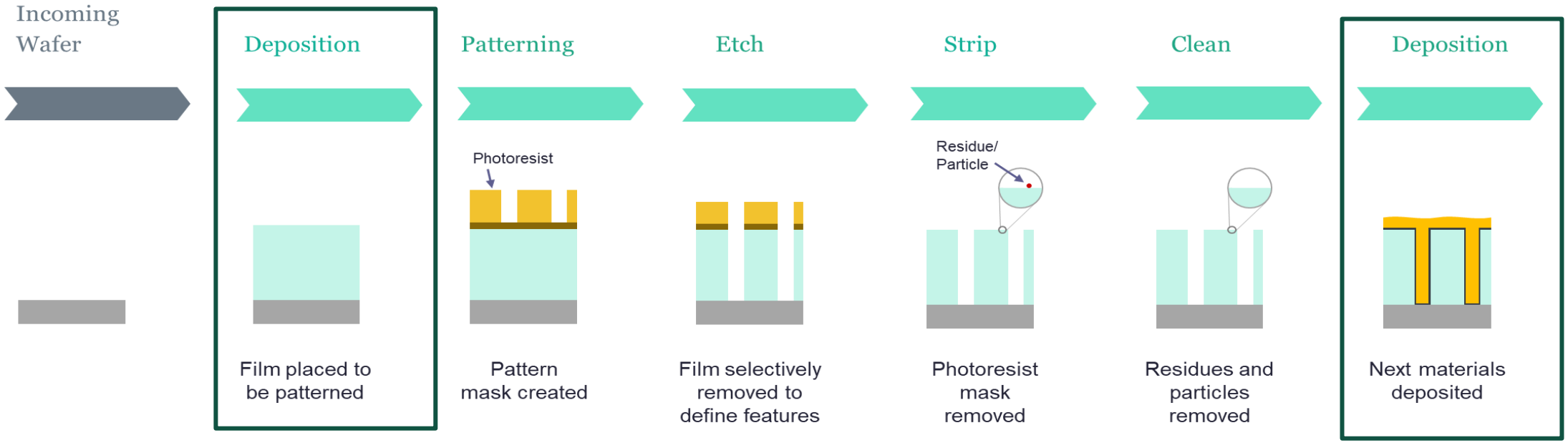


https://sst.semiconductor-digest.com/2016/08/evolution-of-across-wafer-uniformity-control-in-plasma-etch/

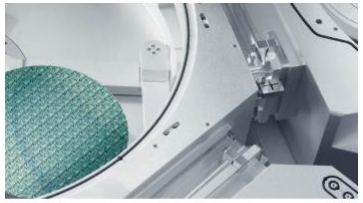
03

Technology and challenges in deposition

Deposition Engineering at Lam Research



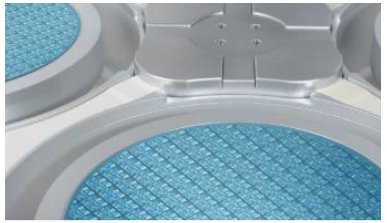
Lam's Deposition Product Portfolio



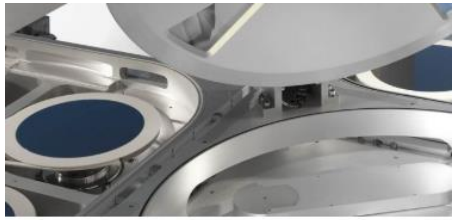
ALTUS Product Family

Reliant Deposition Products

SPEED Product Family



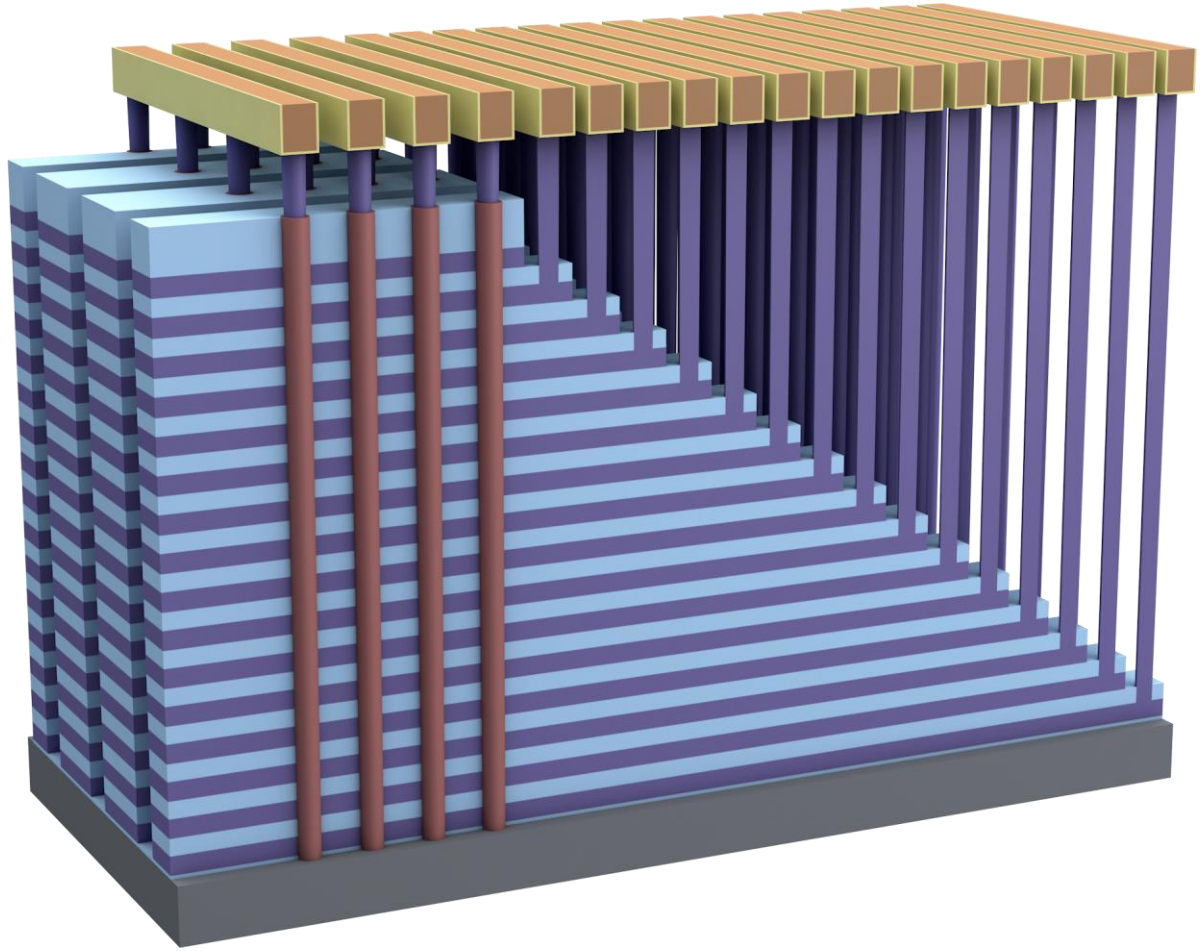
Striker Product Family



VECTOR Product Family

Source: Lam Generated

Deposition processes in 3D NAND



Typical plasma-based deposition processes

Two main branches, similar physics executed differently

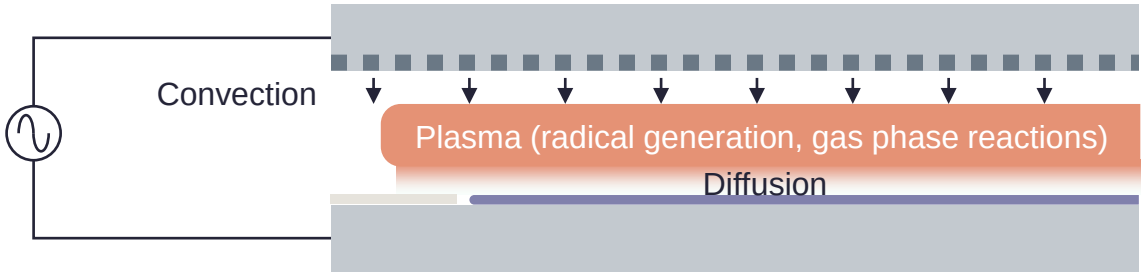
- **PECVD** – plasma enhanced chemical vapor deposition
- **PEALD** – plasma enhanced atomic layer deposition

Many physical processes contribute to final film

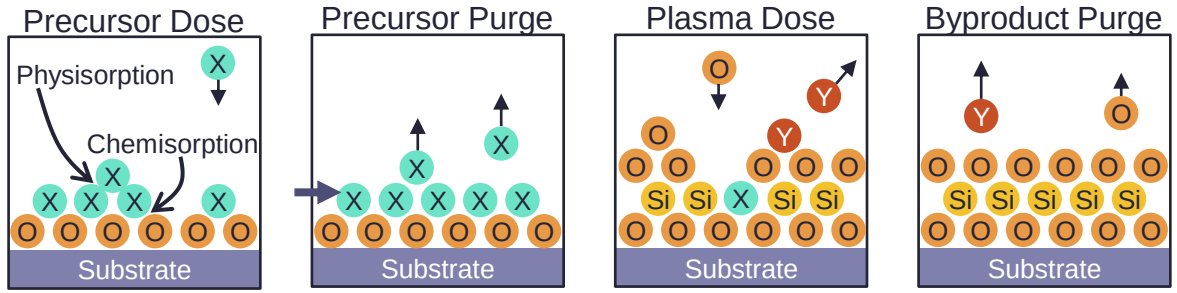
- **Non-equilibrium chemistry**
- **Electrodynamics**
- Fluid transport
- Thermal transport
- Surface kinetics

Gas pressure	~1 Torr to >10 Torr
Gas temperature	~200°C to >500°C
Inter-electrode gap	~5mm to 15mm
Gas mean free path	~10μm to 100μm
Gas species	He, Ar, N_2, O_2, H_2, NH_3, SiH_4, TEOS, ...

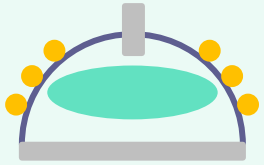
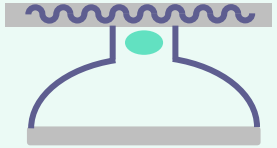
Plasma-enhanced chemical vapor deposition (PECVD)



Plasma-enhanced atomic layer deposition (PEALD)

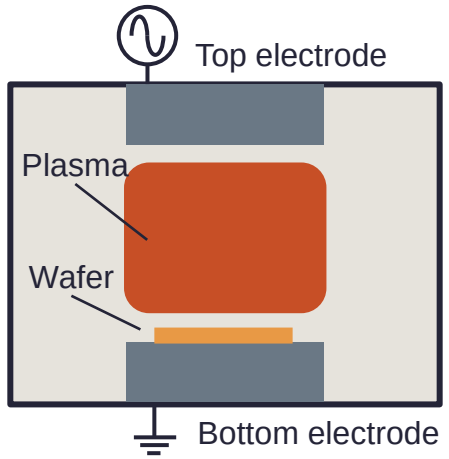


Plasma sources used in deposition

	Capacitively-coupled (CCP)	Inductively-coupled (ICP)	Wave-coupled (MW)
			
Frequency	Up to ~100 MHz	Up to ~100 MHz	Up to 100 GHz
Pressure range		1-10 Torr	
Uniformity	Excellent	Good	Poor
Max plasma density	Low (< ~10^{17} m^{-3})	Medium (< ~10^{19} m^{-3})	High (< ~10^{20} m^{-3})
Radical generation degree	Low	High	Medium to high
Ion-assisted or remote		Both possible with SHD	
Cost	Low	Medium	High

CCP for PECVD/PEALD: ionization at (pre-)sheath

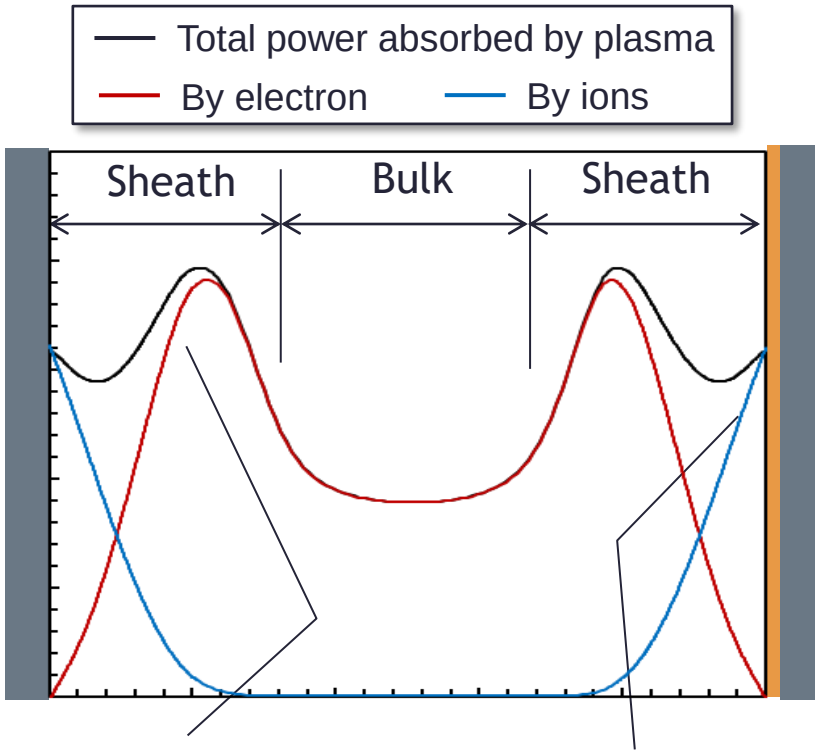
Parallel plate CCP



ASSUMPTION

- 13.56 MHz
- No wall, no edge effect
- Single positive ion species

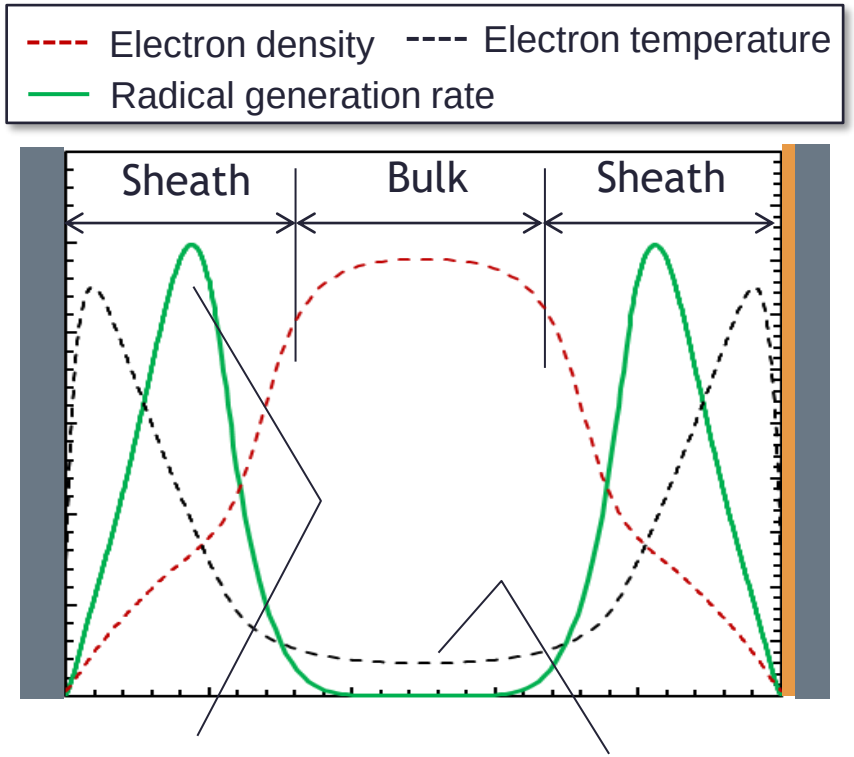
RF power is absorbed in plasma sheath



Electrons are heated in sheath

Ions are heated near surface

Radicals are generated in plasma sheath



Radical generation in sheath

Nothing happens in bulk

Grand challenges: plasma instability

Background

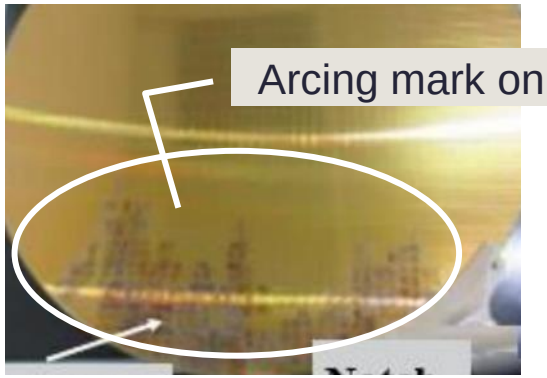
Plasmas react to changing boundary conditions due to deposition and may become unstable.

Wafers exposed to unstable plasmas need to be discarded.

Most are not understood at a predictive level, forces empirical hardware development

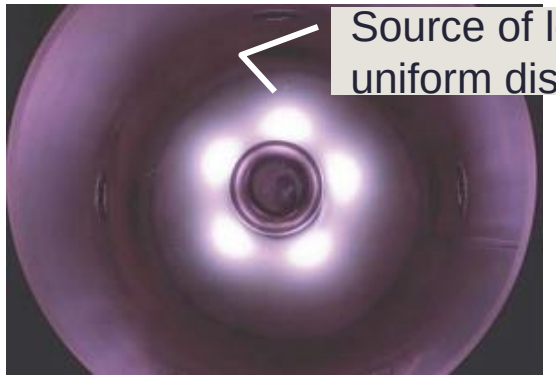
Examples of plasma instabilities observed in PECVD/PEALD

MICRO-ARCING ON WAFER



J.J. Ye, ASMC (2024)

PLASMOID

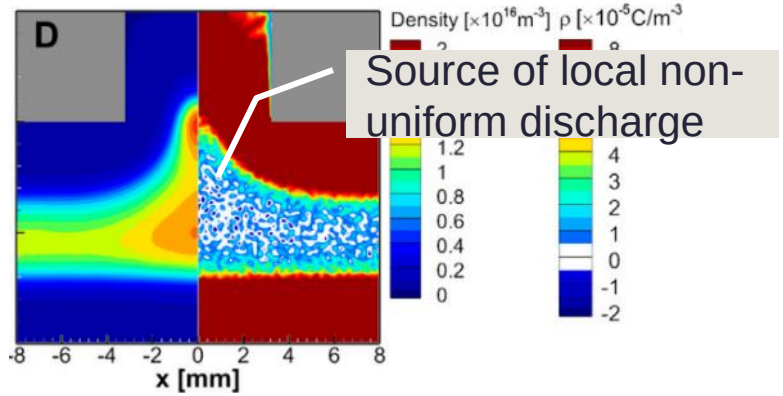


Mackey et al., Appl. Math. Lett. (2005)

CATHODE SPOT

E. Yan, *ECS Transactions*, **18** (2009) 581

HOLLOW CATHODE DISCHARGE



H Park, *Front. Phys.*, **11** (2023) 37994.

Grand challenges: edge uniformity control

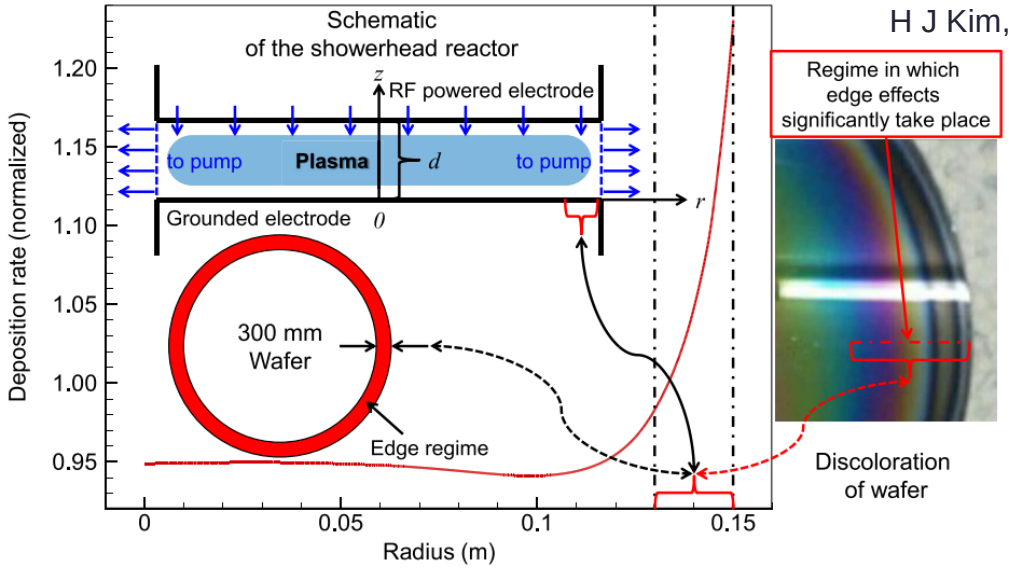
Problem statements

Most customers need thickness uniformity to be < 1%, which typically means a variation of < 1nm or just a few monolayers.

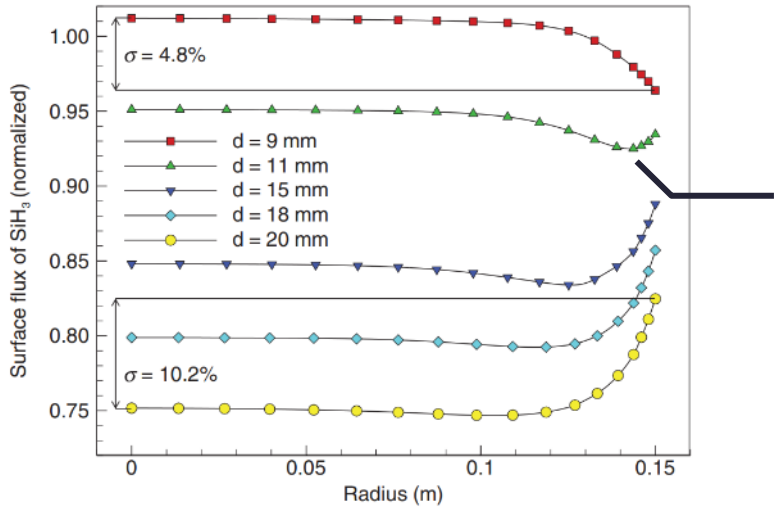
The non-uniformity problem is located near the edge of wafer and electrode due to inherent discontinuities.

Plasma, flow, and temperature are known to cause non-uniformity. However, achieving precise control is challenging due to the non-linear interactions involved.

Examples of edge non-uniformity



H J Kim, *J. Appl. Phys.* **122** (2017) 053301



H J Kim, *Plasma Sources Sci. Technol.* **25** (2016) 065006

Modeling of radical flux on wafer at various electrode gap

There seems to be no solution to achieve <1% uniformity

Grand Challenges: independent control of radicals/ions

Problem statements

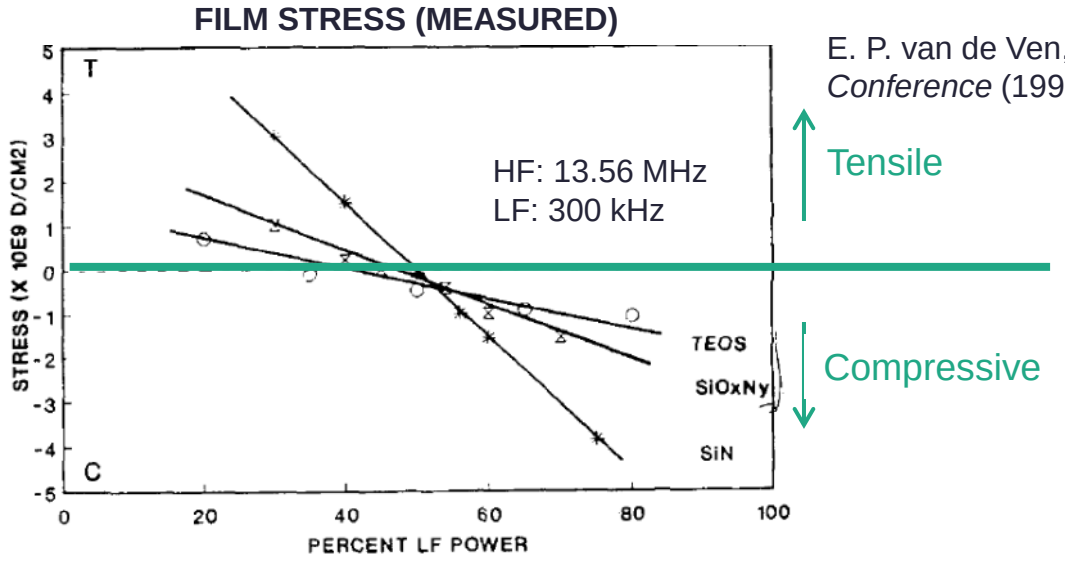
Managing film stress is essential for controlling wafer bow, independent of film thickness

Ions drive film stress, while radicals govern the deposition rate

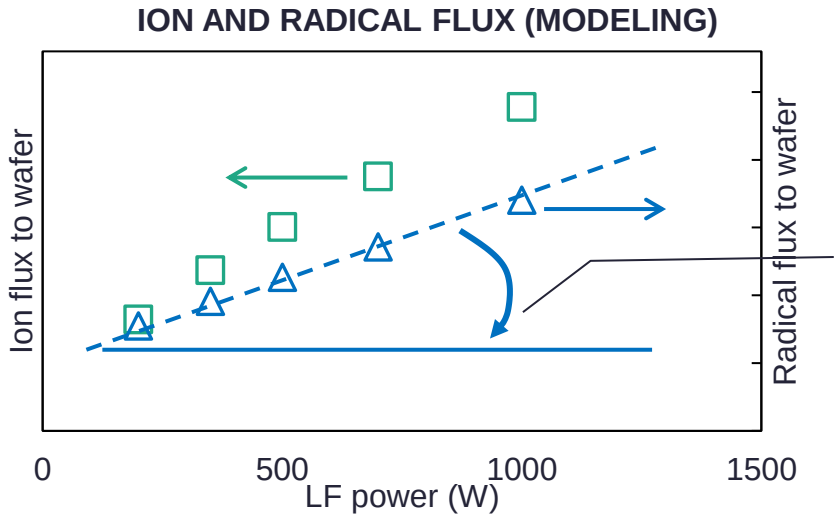
Traditional dual frequency methods cannot independently control ions and radicals

Radical/ion flux	Film stress
High	Tensile
Low	Compressive

Limitation of conventional dual frequency approach



E. P. van de Ven, *Proc. VMIC Conference* (1990)



Ideal case: radical flux is independent of power
How to achieve this?

Grand Challenges: in-situ plasma metrology

Problem statements

Abnormal plasmas and process drift needs to be detected and corrected

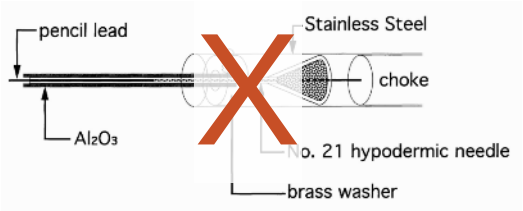
In-situ plasma monitoring is a key to enable AI-assisted automated detection and correction.

However, conventional plasma metrology is not capable of providing critical information.

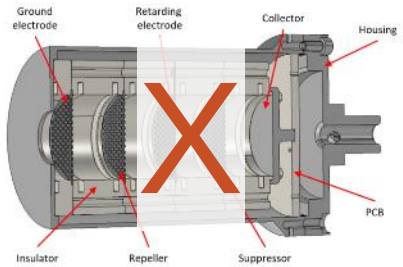
Unique challenges in plasma metrology for PECVD/PEALD

Categories	Requirement
Chemical resistance	F-based and Cl-based chemistry
Thermal resistance	>500°C
Process transparency	No impact to process performance
Temporal information	> 100Hz sampling rate
Spatial information	Resolution higher than 5mm
Pressure	> ~1 Torr

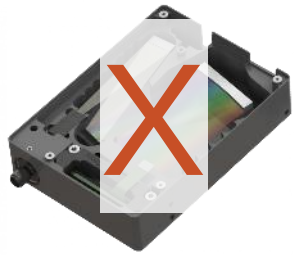
LANGMUIR PROBE



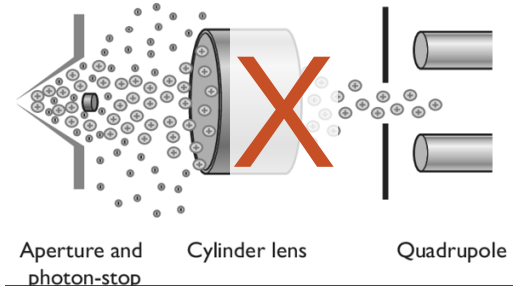
RFEA



OES



MASS SPECTROMETER



Collaboration with academia: U Michigan

Collaborator

- Prof. John Foster, Nuclear Engineering and Radiological Sciences, University of Michigan

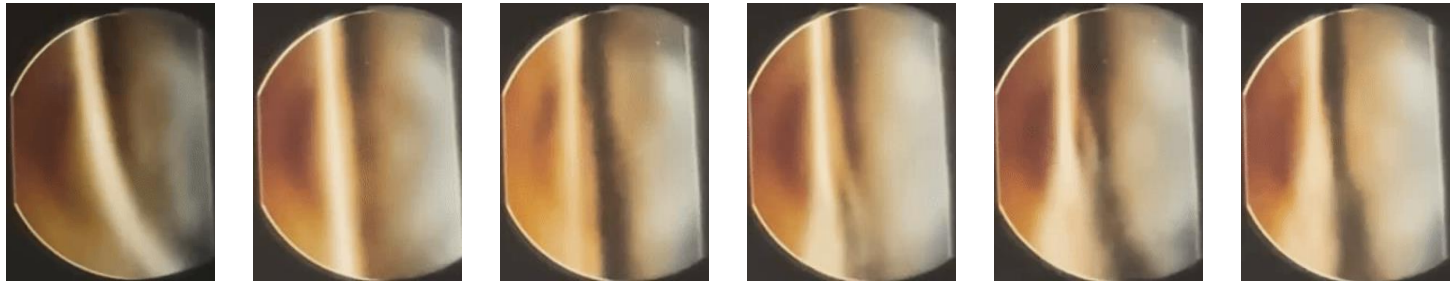
Topic

- Identify methods of stabilizing atmospheric plasma jets in argon

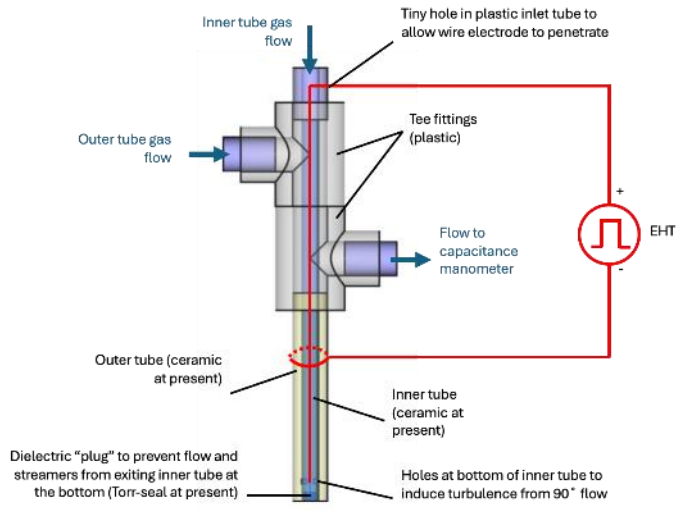
Summary

- Developed unique jet geometry to induce turbulent transport
- Visible imaging has demonstrated significant reduction in filamentation at turbulent conditions

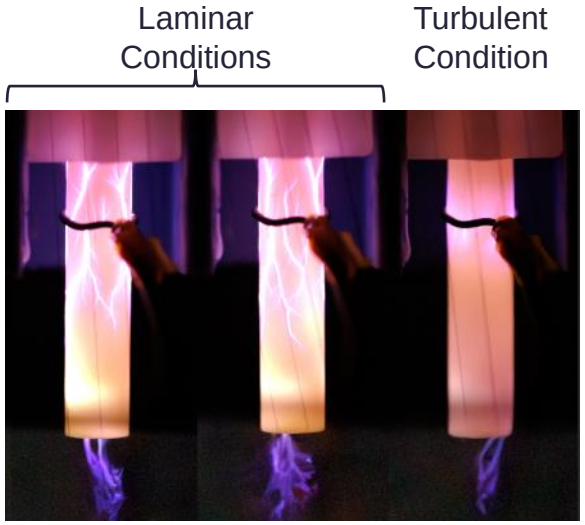
SCHLIEREN IMAGING OF PLASMA JET



SCHEMATIC OF PLASMA JET



VISUAL APPEARANCE OF PLASMA JET



Collaboration with academia: NC State

Collaborator

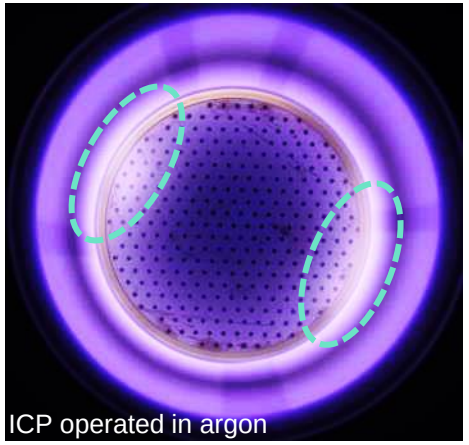
- Prof. Amanda Leitz, Department of Nuclear Engineering, North Carolina State University

Topic

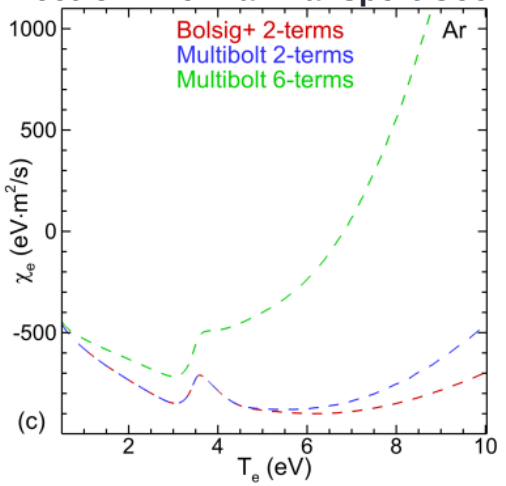
- Understanding of mechanisms of plasma instability
- Development of models to predict unstable conditions

Summary

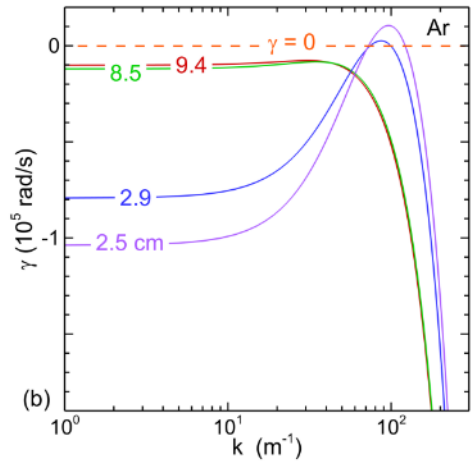
- Demonstrated importance of higher-order Boltzmann solvers for electron thermal transport



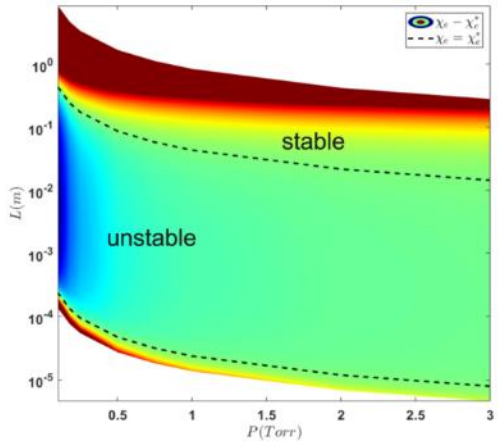
Electron Thermal Transport Coeff.



Dispersion relation for striations



Stability regions for argon ICP



Collaboration with national labs: Sandia

Collaborator

- Dr. Brian Bentz, Sandia National Laboratories

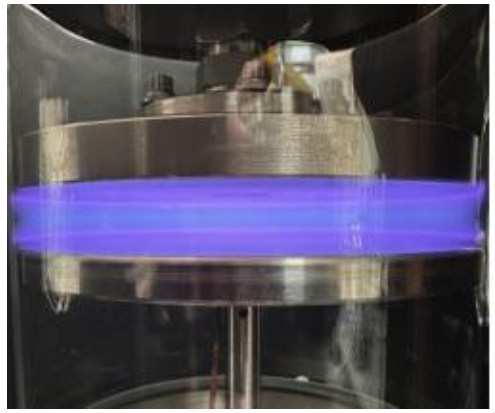
Topic

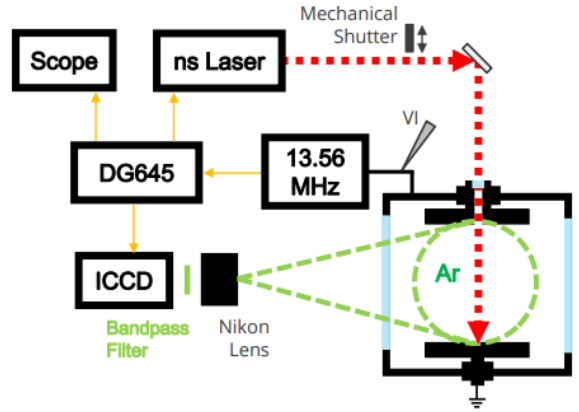
- Fundamental mechanisms of in-situ secondary electron emission from surfaces exposed to plasma

Summary

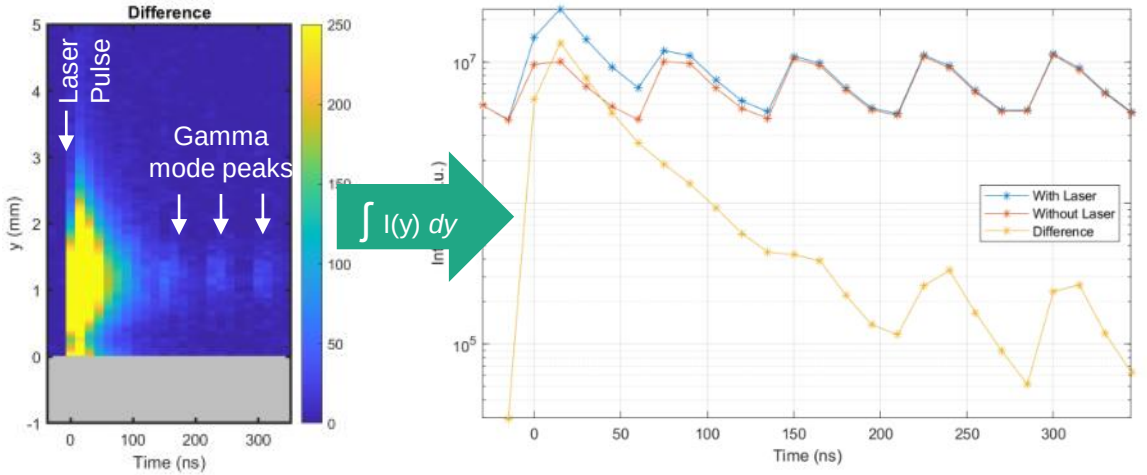
- Completed experimental setup of phase-resolved OES with a UV laser
- Laser turns surface into a momentary photocathode, momentarily increasing ionization and light emission
- Damping of light reflects electron economy at surface

EXPERIMENTAL SETUP WITH PHASE-RESOLVED OES AND UV LASER





DIFFERENCE IN LIGHT INTENSITY BETWEEN WITH AND WITHOUT LASER

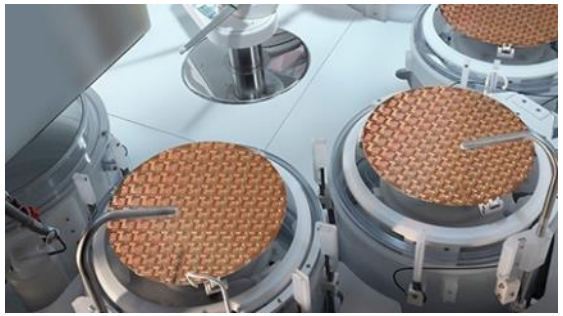


This work was supported by Sandia National Laboratories' Plasma Research Facility, funded by the U.S. Department of Energy Office of Fusion Energy Sciences. Sandia is managed and operated by NTESS under DOE NNSA under DOE NNSA contract DE-NA0003525.

Lam's product portfolio

Enabling technology with high productivity

Deposition



Metal ECD

Ternary PLD

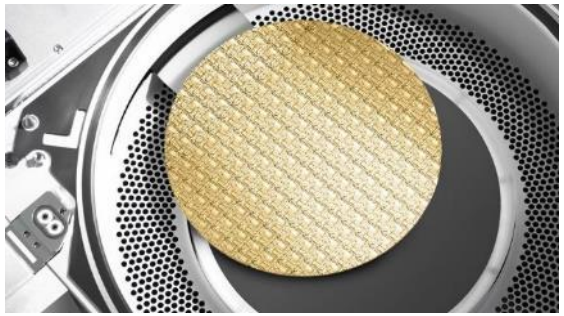
Metal ALD/CVD

Dielectric PECVD

Dielectric ALD

Dielectric HDP-CVD

Etch



Conductor etch

Dielectric etch

Metal etch

Selective etch

TSV etch

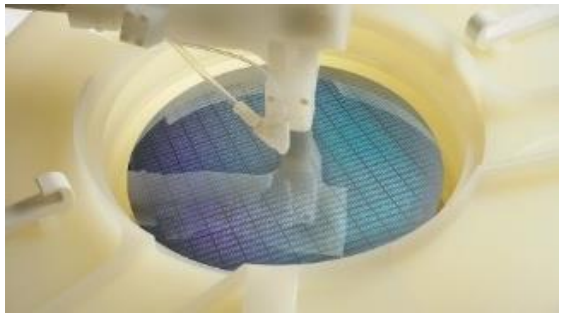
MEMS/Deep Si etch

Strip

Stand-alone strip

Integrated strip

Clean



Spin wet clean

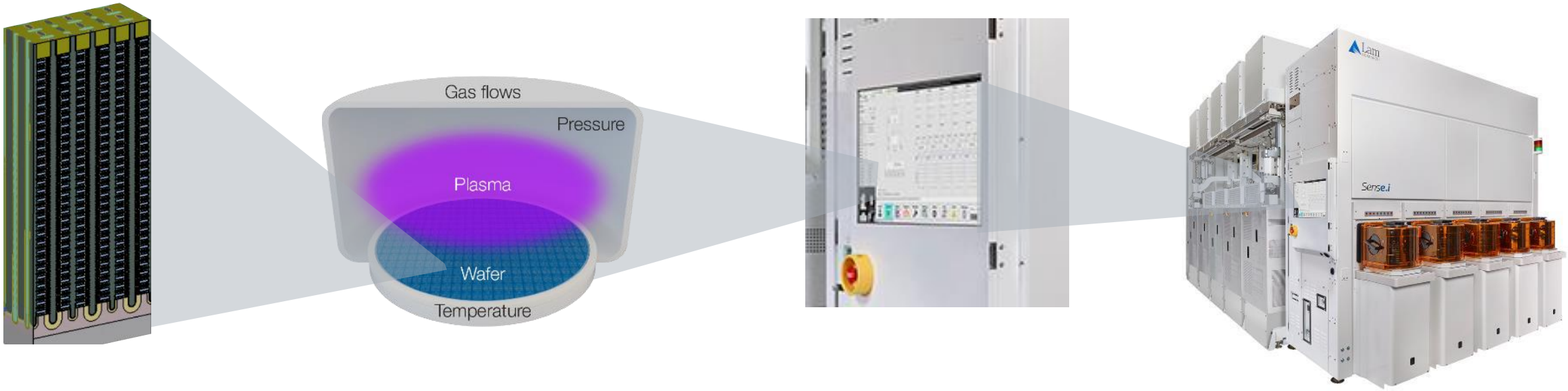
Plasma bevel clean

ALD = atomic layer deposition, CVD = chemical vapor deposition, ECD = electrochemical deposition, HDP-CVD = high density plasma CVD, PECVD = plasma-enhanced CVD, PLD = pulsed laser deposition, TSV = through-Si via

04

Careers at Lam Research

Lam needs expertise in every high-tech discipline



On-Wafer Process

- Chemistry
- Chemical engineering
- Materials engineering
- Surfaces and interfaces

Sub-Systems

- Circular chemical, energy, and water management
- Chamber materials
- RF/Plasma technology
- Pressure control
- Temperature control
- Electrical Engineering
- Mechanical Engineering

Software and Control

- Algorithms
- Analytics
- Computing and networking
- Data management
- Modeling and simulation
- Sensors
- Timing
- User experience

System

- Adaptivity
- Architecture
- Automation
- Manufacturability
- Reliability
- Mechatronics
- Self-awareness
- Self-maintenance
- Serviceability

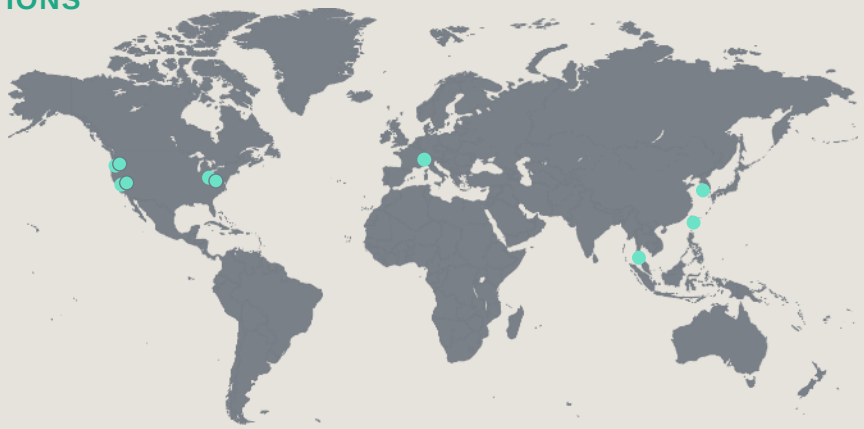
Lam RESEARCH

A global leader in wafer fabrication equipment and services since 1980

$14.3B	$1.7B	~17,200
REVENUE*	R&D*	EMPLOYEES*

10 PRIMARY LOCATIONS

+ Fremont, CA
+ Livermore, CA
+ Sherwood, OR
+ Tualatin, OR
+ Springfield, OH
+ Eaton, OH
+ Villach, Austria
+ Gyeonggi-do, Korea
+ Taoyuan City, Taiwan
+ Batu Kawan, Malaysia



RECENT AWARDS AND RECOGNITION

World's Most Admired Companies
Fortune

America's Most Responsible Companies
Newsweek

World's Top Female-Friendly Companies
Forbes

Best Places to Work For LGBTQ+ Equality
Human Rights Campaign

100 Most Sustainable U.S. Companies
Barron's

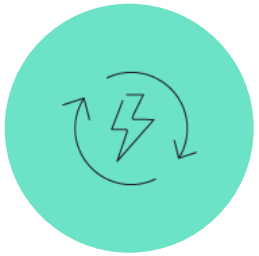
Dow Jones Sustainability Index North America
S&P Global

*Figures as of calendar year 2023.

Our strengths set us apart

Collaboration

Together we're stronger and smarter



Innovation

We solve the unsolvable

Impact

We're a catalyst for global advancement

Recent awards and recognition

World's Most Admired Companies Fortune	**America's Most Responsible Companies** Newsweek	**World's Top Female-Friendly Companies** Forbes
Best Places to Work for LGBTQ+ Equality Human Rights Campaign	**100 Most Sustainable U.S. Companies** Barron's	**Dow Jones Sustainability Index North America** S&P Global

Future opportunities at Lam Research

Full-time Roles – Bachelor's, Master's and PhD level

- Process Engineers
- Product Engineers
- Electrical Engineers
- Mechanical Engineers
- Manufacturing Engineers
- Test Engineers
- Software Engineers
- Hardware Engineers

Majors Lam Research typically recruits for			
Chemical Engineering	Chemistry	Mechanical Engineering	Electrical Engineering
RF Engineering	Materials Science	Industrial Engineering	Supply Chain
Physics	Data Science	AI/Machine Learning	Business Functions

Internships – Bachelor's, Master's and PhD level

- Get hands on business experience that complements your academic studies and prepares you for real-world situations
- We hire interns each summer across our US offices (Tualatin, OR as well as Fremont and Livermore, CA)
- Relocation stipend is provided to students who go to school that is more than 50 miles from the office they will complete their internship in
- The intern program takes place during the summer with internships lasting ~12 weeks

Interested in learning more?

- Check out our career page: www.lamresearch.com/careers/

Scan QR code to submit resume to recruiting team

Q&A